MM1001 LDMOS TRANSISTOR

Document Number: MM1001
Product Datasheet V4.0

10W, 28V High Power RF LDMOS FETs

Description

The MM1001 is a 10-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies up to 2 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

MM1001

- Typical Performance (On Innogration fixture with device soldered):
  V_{DD} = 28 Volts, I_{DQ} = 100 mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	η_D@P_{-1} (%)
960 MHz	23	13	63

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					

Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	90	97		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 50 μA)	$V_{GS}(th)$	——	2.07	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		16.2		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		5.9		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		0.5		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 100mA, f = 960 MHz, CW Signal Measurements.

Power Gain	G_p	——	23	——	dB
Drain Efficiency@P1dB	η_D	——	63	——	%
1 dB Compression Point	P_{-1dB}	——	13	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 960 MHz

VSWR 20:1 at 13W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

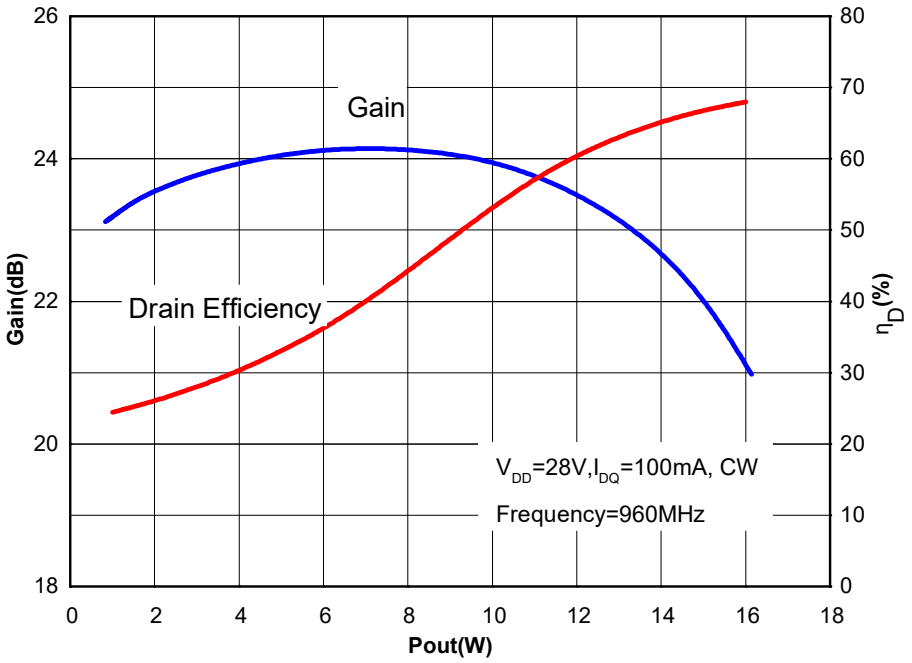


Figure 1. Power gain and drain efficiency as function of Power out

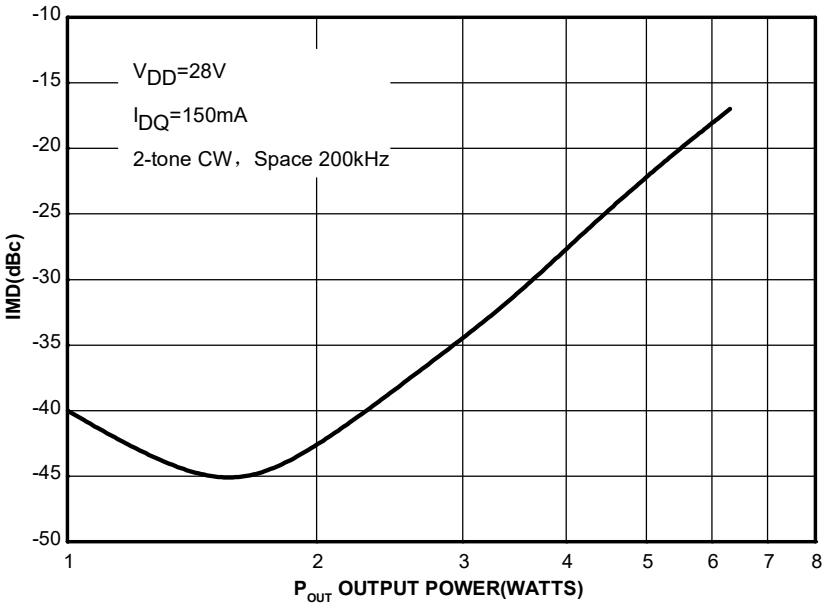
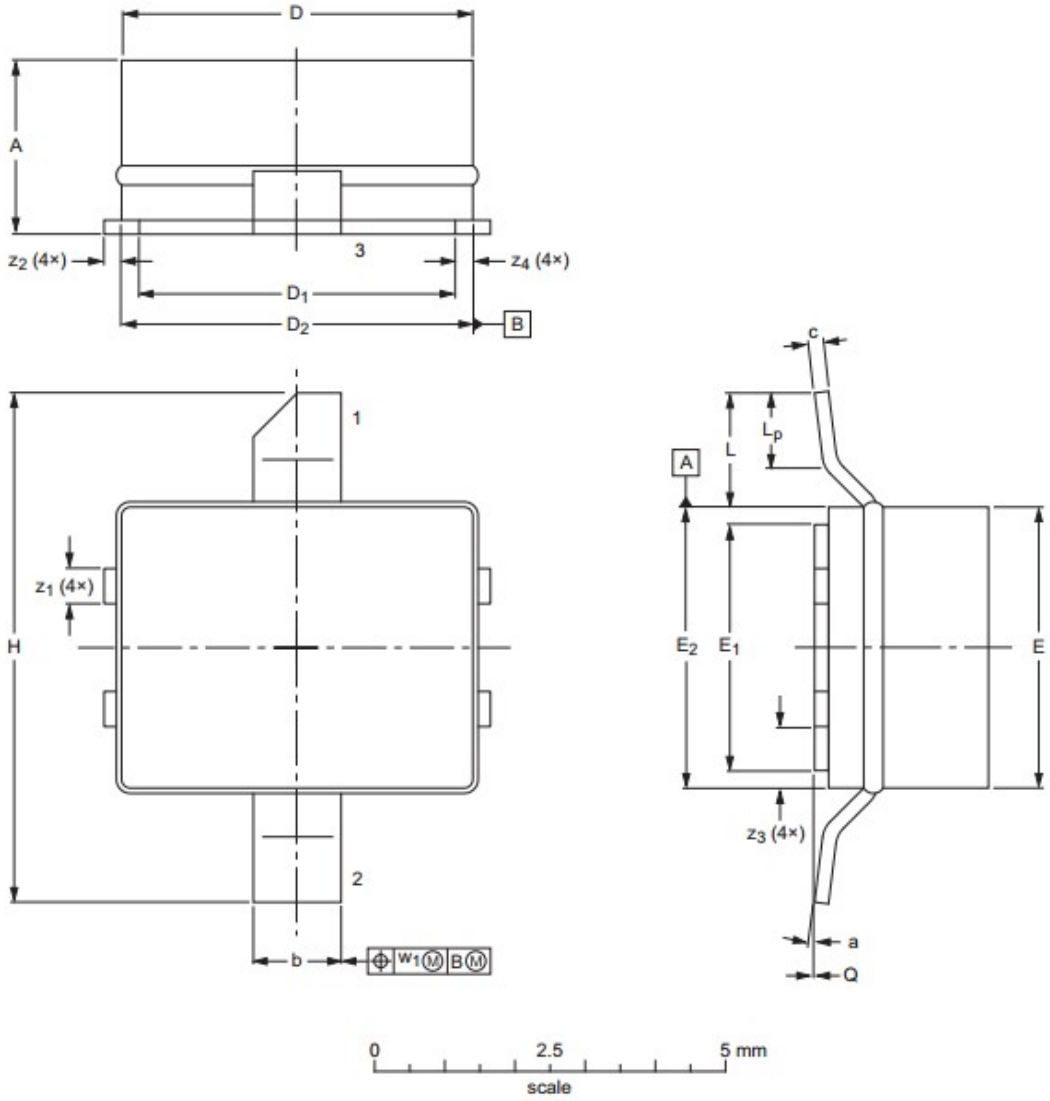


Figure 2. IMD3 versus Output Power

Package Outline

Earless Flanged ceramic package; 2 leads(1-Drain,2-Gate,3-Source)



UNIT	A	b	c	D	D_1	E	E_1	E_2	H	L	L_P	Q	w_1	z_1	z_2	z_3	z_4	α
mm	2.34	1.35	0.23	5.16	4.65	4.14	3.63	4.14	7.49	2.03	1.02	0.1	0.25	0.58	0.25	0.97	0.51	7°
	2.13	1.19	0.18	5.00	4.50	3.99	3.48	3.99	7.24	1.27	0.51	0.0		0.43	0.18	0.81	0.00	0°

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-MM					18/6/2014

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2015/4/29	**Rev 1.0**	**Preliminary Datasheet**
2016/8/8	**Rev 2.0**	**Preliminary Datasheet**
2016/11/23	**Rev 3.0**	**Preliminary Datasheet**
		Add test data and graph
2016/12/27	**Rev 3.1**	**Preliminary Datasheet**
		Add Thermal Resistance
2017/02/22	**Rev 4.0**	**Product Datasheet**
		Add CV parameter

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