

MQ1080VP LDMOS TRANSISTOR

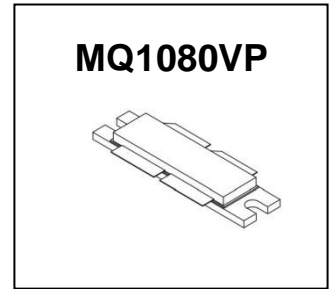
Document Number: MQ1080VP
Preliminary Datasheet V1.0

800W, 50V High Power RF LDMOS FETs

Description

The MQ1080VP is a 800-watt, high performance, internally matched LDMOS FET, designed for multiple applications with frequencies 0.5 to 1GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as UHF TV and Aerospace applications.



•Typical Performance (on 650MHz test fixture with device soldered):

Test signal: Pulse CW pulse width: 100us, duty cycle:10%, VDD = 50 Volts, IDQ = 200 mA, TA = 25 C

Frequency	Gp (dB)	P _{OUT} (W)	$\eta_D@P_{OUT}$ (%)
650 MHz	16	800	67

Suitable Applications

- 470-860MHz (TV UHF)
- 650MHz particle accelerator
- 915MHz RF Energy industry application
- Wideband Lab power amplifier
- High power intermodulation tester

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	125	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 800W Pulse CW, 50 Vdc, IDQ = 100mA 650MHz	R _{θJC}	0.16	°C/W

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =1uA)	V _{DSS}		122	---	V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50 V, V _{GS} = 0 V)	I _{DSS}	---	---	10	μA
Gate--Source Leakage Current (V _{GS} = 6 V, V _{DS} = 0 V)	I _{GSS}	---	---	1	μA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 uA)	V _{GS(th)}	---	1.6	---	V
Gate Quiescent Voltage (V _{DD} = 50 V, I _{DQ} = 100 mA, Measured in Functional Test)	V _{GS(Q)}	2.1	2.6	3.1	V

Functional Tests (In Innogration Demo-650MHz, 50 ohm system) :V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f = 650 MHz, Pulse CW Signal Measurements. (Pulse Width=100 μs, Duty cycle=10%)

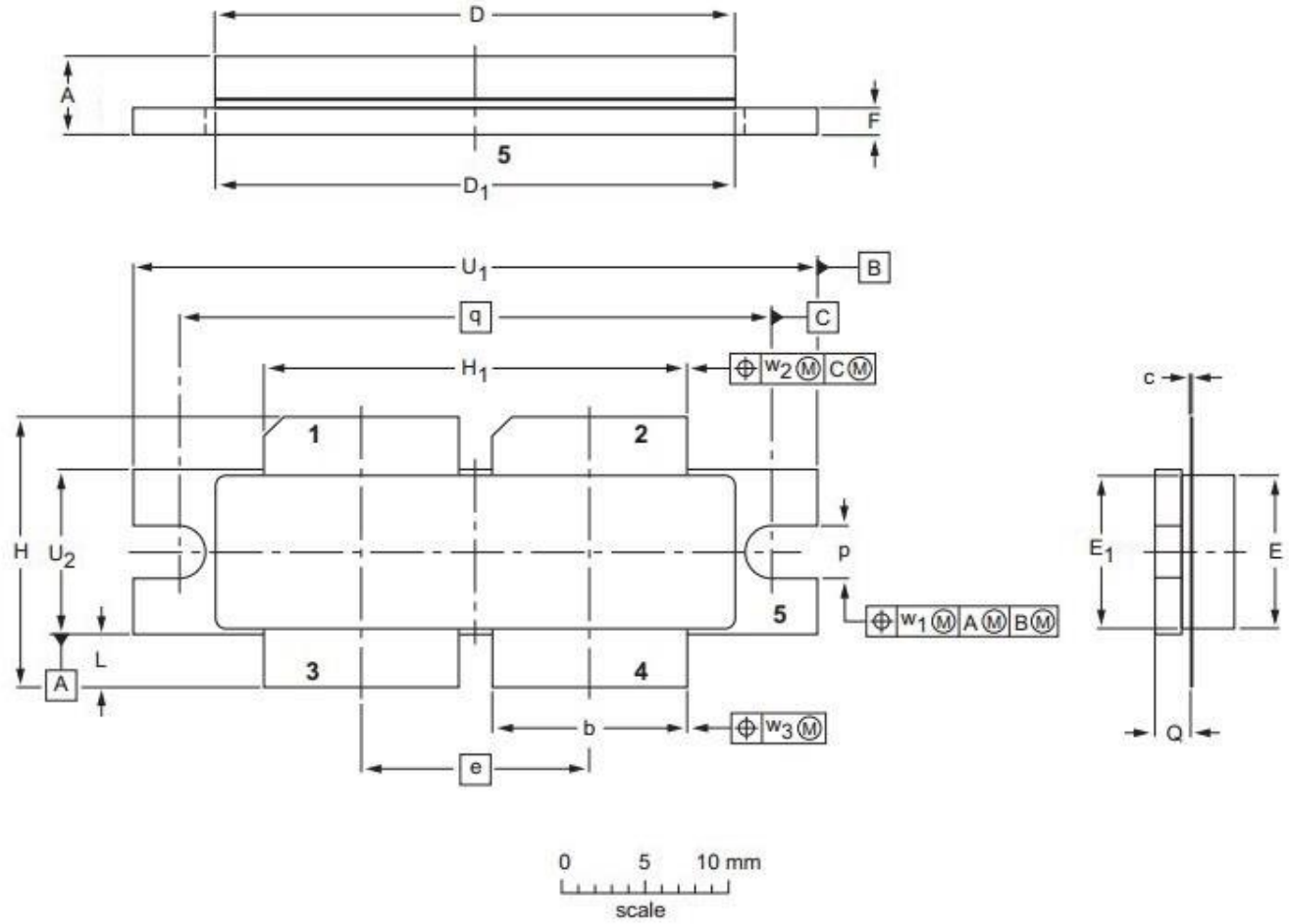
Power Gain	G _p	---	16	---	dB
Output Power	P _{out}	---	800	---	W
Drain Efficiency@P1dB	η _D	---	67	---	%
Input Return Loss	IRL	---	-5	---	dB

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2017/07/19	Rev 1.0	Preliminary Datasheet Creation

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