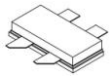
1300MHz-1600MHz, 180W, 28V High Power RF LDMOS FETs

Description

The ITCH16180B4 is a 180-watt, internally matched LDMOS FET, designed for multicarrier WCDMA/PCS/DCS/LTE base station and ISM applications with frequencies from 1300 to 1600 MHz. Four leads can be configured as single ended, 180 degree push-pull or 90 degree hybrid or Doherty with proper external match network.

ITCH16180B4



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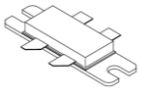


- Typical Class AB Performance of Single Section (On Test Fixture with device soldered):

VDD = 28 Volts, I_{DQ} = 700 mA, Pulse CW, Pulse Width=12 us, Duty cycle=10% .

Frequency	Gp (dB)	P_{-1dB} (dBm)	η_D@P_{-1} (%)	P_{-3dB} (dBm)	η_D@P_{-3} (%)
1447 MHz	19.9	49.1	54.8	50.1	57.9
1457 MHz	20.0	48.8	54.5	49.8	57.6
1467 MHz	20.0	48.3	53.5	49.4	56.7

- Typical Performance of Doherty Circuit(On Test Fixture with device soldered):

V_{DD} = 28 Volts, I_{DQMAIN} = 700 mA, V_{GPEAK}=1.3V, Pulse CW, Pulse Width=12 us, Duty cycle=10% .

Frequency	Gp (dB)	P_{-1dB} (dBm)	η_D@P_{-1} (%)	P_{-3dB} (dBm)	η_D@P_{-3} (%)
1447 MHz	18.1	50.6	53.2	53.1	58.3
1457 MHz	18.0	50.5	52.5	53.0	58.3
1467 MHz	18.0	50.3	51.8	52.9	58.3

- Typical Single-Carrier W-CDMA Performance of Doherty Circuit (On Test Fixture with device soldered):

V_{DD}=28Volts, I_{DQMAIN} = 700 mA, V_{GPEAK}=1.3V, P_{out}= 44.5dBm Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 10.5 dB @ 0.01% Probability on CCDF.

Frequency	P_{OUT}（dBm）	Gp (dB)	η_D (%)	$ACPR_{5M}$ (dBc)	$ACPR_{10M}$ (dBc)
1447 MHz	44.5	17.9	40.8	-32.7	-53.5
1457 MHz	44.5	17.8	40.6	-34.0	-54.1
1467 MHz	44.5	17.7	40.3	-35.3	-54.5

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Optimized for Doherty Applications
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	70	Vdc

Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 87°C, T_J=175°C, DC test, Dissipation Power 85W	RθJC	0.52	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics（per Section）					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	65	70		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			100	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 450 uA)	$V_{GS(th)}$	1.5	2.0	2.5	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_{DQ} = 700 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.8		V
Functional Tests of per Section (On Production Test Fixture, 50 ohm system) : V_{DD} = 28 Vdc, I_{DQ} = 700 mA, f = 1457 MHz, Pulse CW, Pulse Width=12 us, Duty cycle=10% .					
Power Gain（Maximum Gain）	Gp	18.5	19.7		dB
Drain Efficiency@P3dB	η_D	52	55		%
1 dB Compression Point	P_{-1dB}	47.5	49		dBm
3dB Compression Point	P_{-3dB}	48.5	50		dBm
Input Return Loss	IRL		-10		dB

Load Mismatch of per Section (On Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 700 mA, f = 1467 MHz

VSWR 10:1 at 87W pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

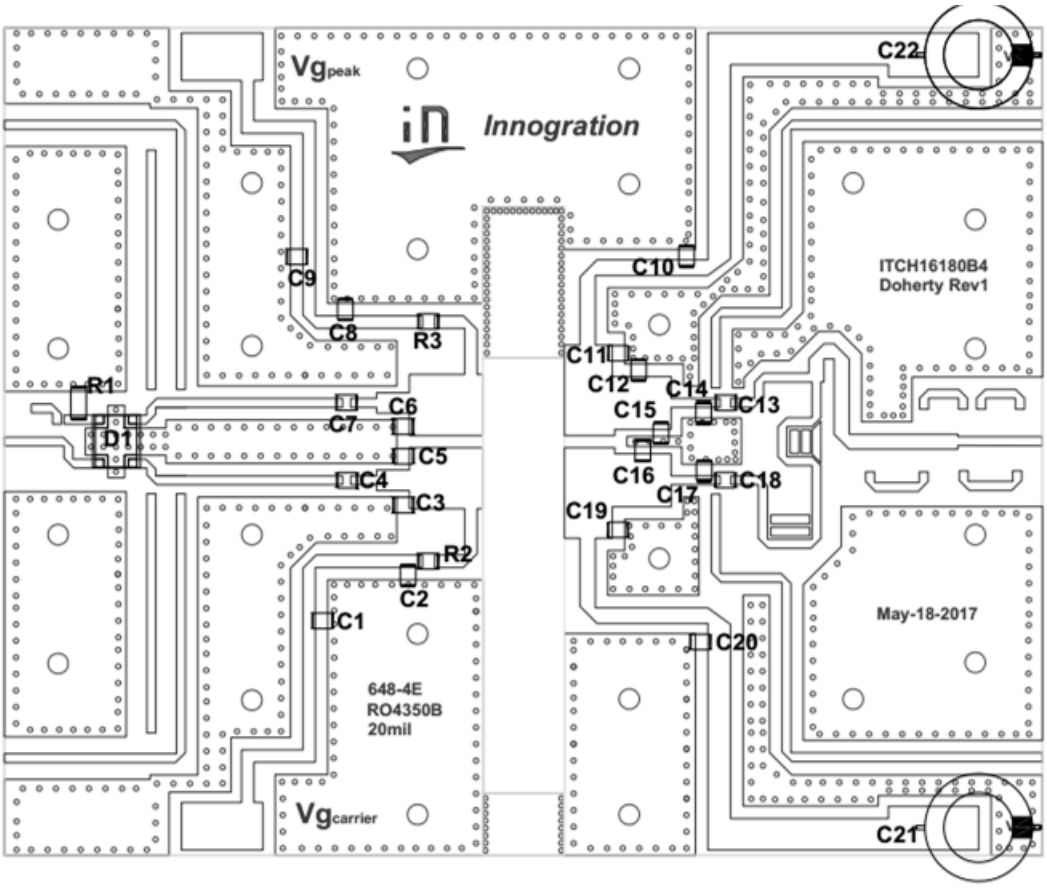


Figure 1. Test Circuit Component Layout (1447MHz~1467MHz)

Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer	P/N
C2,C8,C13,C18	Ceramic Capacitor,28pF	ATC	600F 280
C3,C16	Ceramic Capacitor,3.3pF	ATC	600F 3R3
C4,C7,C11,C19	Ceramic Capacitor,5.6pF	ATC	600F 5R6
C5	Ceramic Capacitor,0.7pF	ATC	600F 0R7
C6,C14,C15,C17	Ceramic Capacitor,2.7pF	ATC	600F 2R7
C12	Ceramic Capacitor,1.0pF	ATC	600F 1R0
C1,C9,C10,C20	10uF 100V chip Capacitor		
C21,C22	Electrolytic Capacitor ,220uF,63V		
D1	Spliter		
R1	50Ω 4W Chip Resistor		
R2,R3	Chip Resistor,10Ω		
PCB	0.508mm [0.020"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper		

TYPICAL CHARACTERISTICS

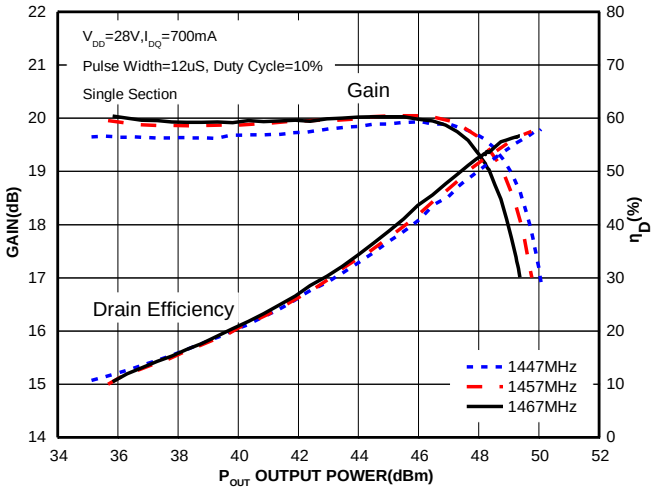


Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power（Single Section On Test Fixture）

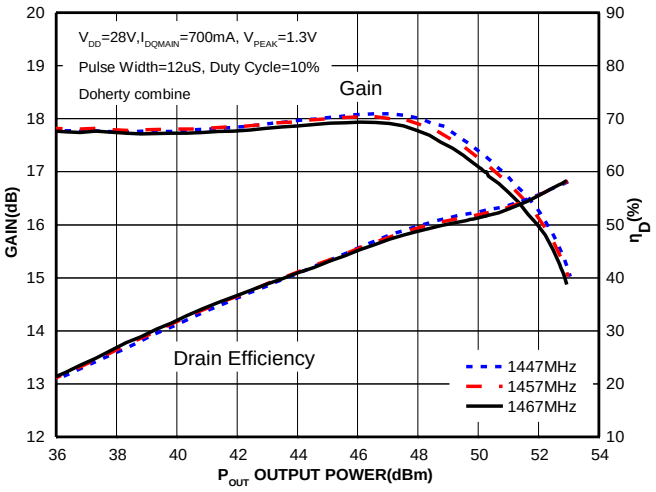


Figure 3. Power Gain and Drain Efficiency as Function of Pulse Output Power（On Doherty Test Fixture）

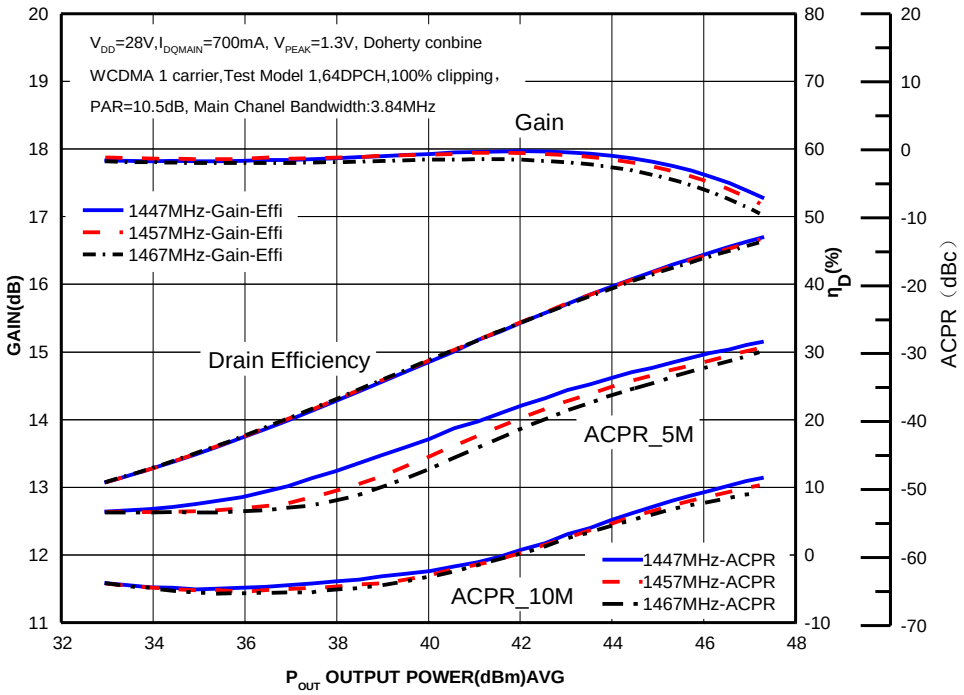


Figure 4. Single−Carrier WCDMA Power Gain and Drain Efficiency and ACPR at 5 MHz and at 10 MHz as Function of Average Output Power（On Doherty Test Fixture）

Table 6. Single Section Load-Pull Performance：

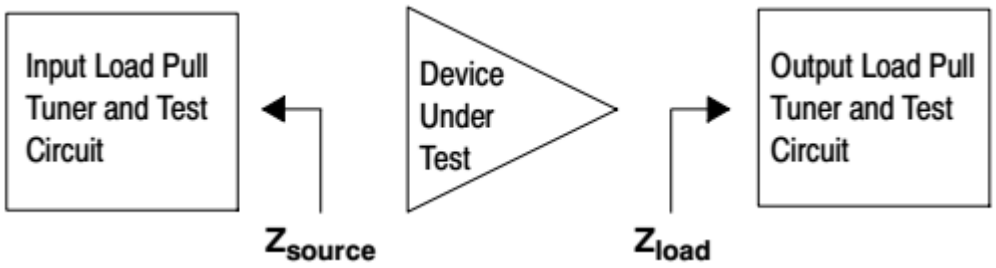
V_{DD} = 28 Vdc, I_{DQ} = 700 mA, Pulsed CW, Pulse Width=200 us, Duty cycle=20% .

f (MHz)	Tuning Type	Z_{source} (Ω)	P1dB				P3dB			
			Z_{load} (Ω)	P1dB (dBm)	Gain (dB)	η_D (%)	Z_{load} (Ω)	P3dB (dBm)	Gain (dB)	η_D (%)
1447	Max Output Power	2.9-j*6.9	1.3-j*2.2	50.3	19.3	58.2	1.4-j*2.3	51.3	17.2	61.4
	Max Drain Efficiency	2.9-j*6.9	1.3-j*1.2	48.7	21.6	65.3	1.3-j*1.3	49.8	19.4	68.0
	Trade Off	2.9-j*6.9	1.3-j*1.9	50.1	20.1	60.7	1.5-j*1.9	51.1	18.1	64.0
1457	Max Output Power	3.2-j*6.5	1.3-j*2.2	50.2	19.4	58.1	1.4-j*2.3	51.2	17.2	60.6
	Max Drain Efficiency	3.2-j*6.5	1.2-j*1.3	48.7	21.6	65.2	1.2-j*1.3	49.6	19.5	67.6
	Trade Off	3.2-j*6.5	1.3-j*1.9	50.0	20.1	60.6	1.5-j*2.0	51.0	18.0	63.2
1467	Max Output Power	3.8-j*6.0	1.3-j*1.6	50.1	19.4	59.5	1.4-j*1.8	51.1	17.1	61.8
	Max Drain Efficiency	3.8-j*6.0	1.2-j*0.9	48.8	21.3	64.4	1.2-j*0.9	49.9	19.2	67.9
	Trade Off	3.8-j*6.0	1.2-j*1.3	49.9	20.2	61.7	1.3-j*1.4	50.9	18.0	64.1

Note：

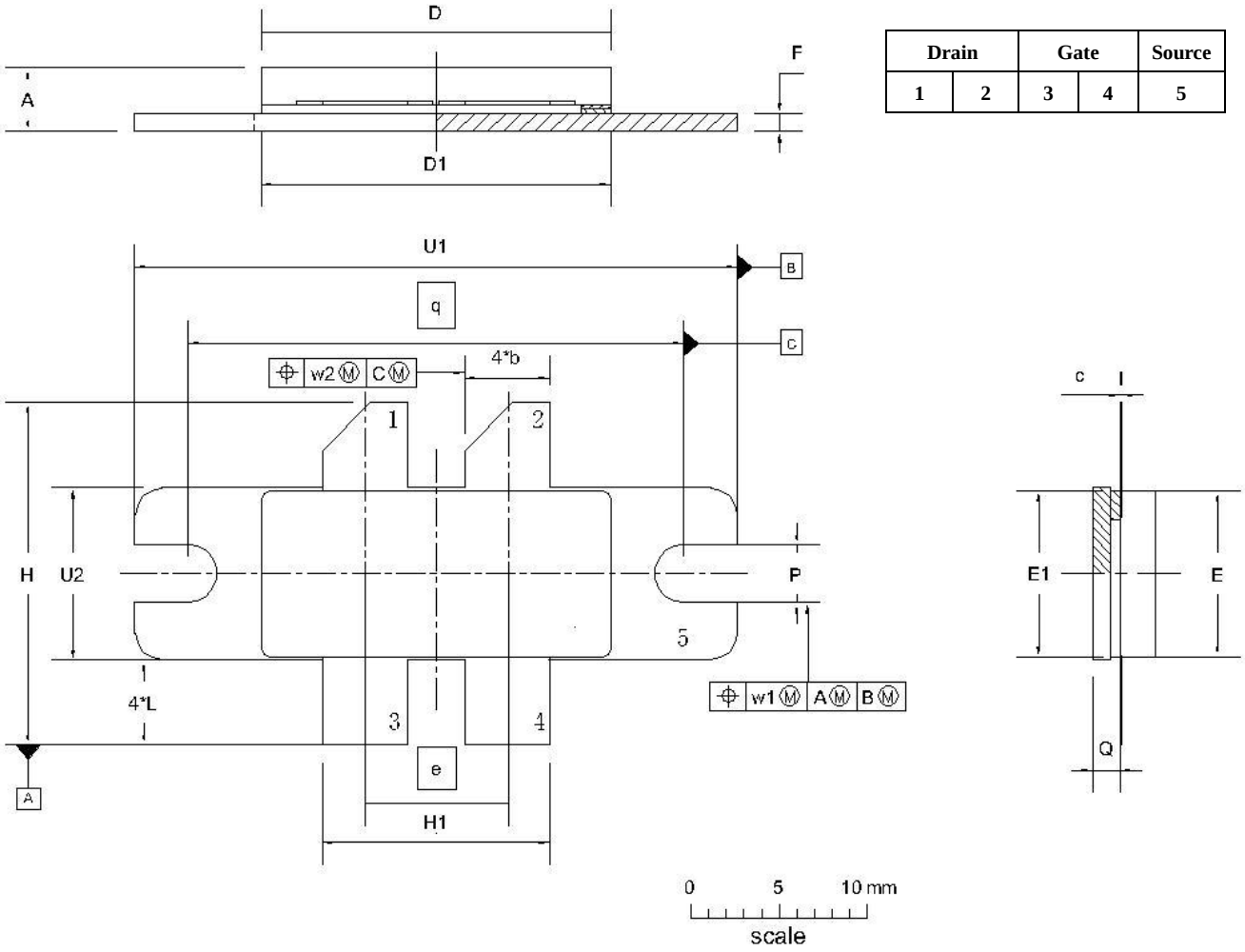
Zsource = Measured impedance presented to the input of the device at the package reference plane.

Zload = Measured impedance presented to the output of the device at the package reference plane.



Package Outline

Eared Flanged Ceramic Package; 2 mounting holes; 4 leads

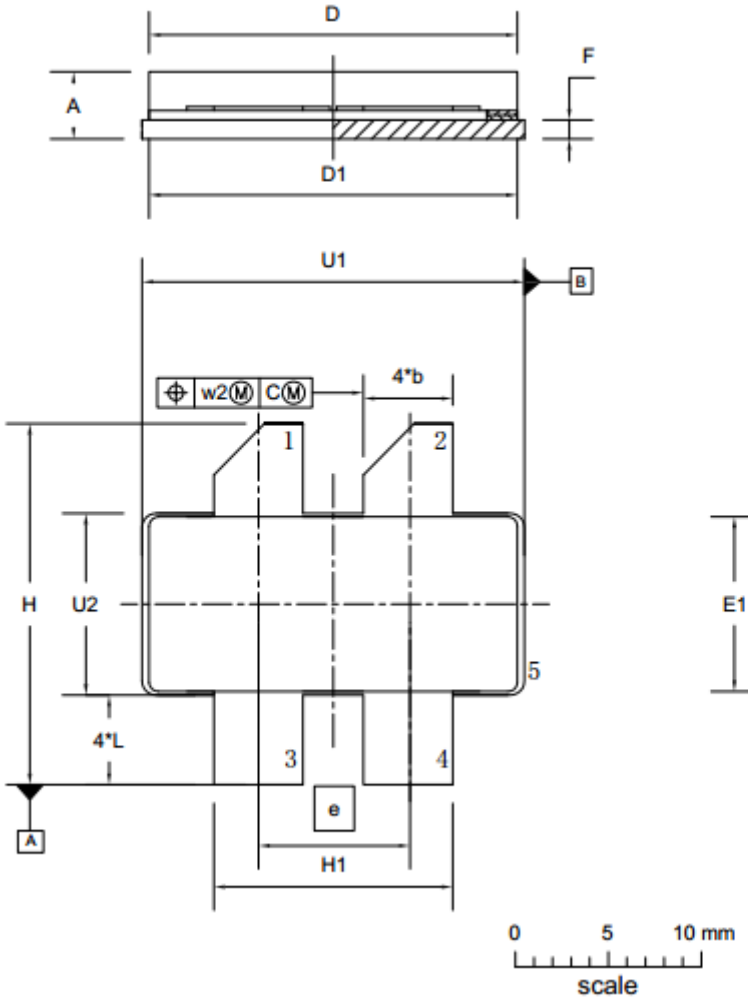


Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2017/02/07	Rev 1.0	Preliminary Datasheet
2017/07/12	Rev 2.0	Product Datasheet

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