



## 700MHz-3600MHz, 20W, 28V RF Power LDMOS FETs

### Description

The ITCH36015E2 is a 20-watt, internally matched LDMOS FET, designed for cellular base station and ISM applications with frequencies from 700MHz to 3600 MHz

### ITCH36015E2



•Typical Performance (On Innogrator fixture with device soldered):

$V_{DD} = 28$  Volts,  $I_{DQ} = 120$  mA, Pulse Width =20us, Duty Cycle =10%.

Frequency (MHz)	$G_{MAX}$ (dB)	P_1dB (dBm)	P_3dB (dBm)	$\eta_D$ (%)	P <sub>avg</sub> =33dBm WCDMA Signal <sup>(1)</sup>		
					Gp (dB)	$\eta_D$ (%)	ACPR_5M (dBc)
869	22.9	43.7	44.2	64.1	22.6	21.6	-37.1
881.5	22.9	43.4	44.0	65.7	22.5	22.2	-38.8
894	22.4	43.2	43.7	67.2	22.2	22.9	-39.4

•Typical Performance (On Innogrator fixture with device soldered):

$V_{DD} = 28$  Volts,  $I_{DQ} = 100$  mA, Pulse Width =20us, Duty Cycle =10%.

Frequency (MHz)	$G_{MAX}$ (dB)	P_1dB (dBm)	P_3dB (dBm)	$\eta_D$ (%)	P <sub>avg</sub> =33dBm WCDMA Signal <sup>(1)</sup>		
					Gp (dB)	$\eta_D$ (%)	ACPR_5M (dBc)
2500	15.4	44.3	44.9	57.7	14.7	19.9	-36.4
2600	16.4	43.8	44.4	59.7	15.9	21.7	-37.2
2700	15.6	42.9	43.6	57.8	15.0	23.4	-37.2

•Typical Performance (On Innogrator fixture with device soldered):

$V_{DD} = 28$  Volts,  $I_{DQ} = 140$  mA, Pulse Width =20us, Duty Cycle =10%.

Frequency (MHz)	$G_{MAX}$ (dB)	P_1dB (dBm)	P_3dB (dBm)	$\eta_D$ (%)	P <sub>avg</sub> =32.5dBm WCDMA Signal <sup>(1)</sup>		
					Gp (dB)	$\eta_D$ (%)	ACPR_5M (dBc)
3400	15.8	42.8	44.0	44.0	15.5	14.8	-38.3
3500	16.7	42.6	43.9	48.2	16.6	16.2	-40.3
3600	16.3	41.8	43.3	44.4	16.1	16.2	-41.8

Note(1) WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz, PAR =10.5 dB at 0.01 % probability on CCDF.

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	+65	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc



Operating Voltage	$V_{DD}$	+32	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$ , $T_J = 200^\circ\text{C}$ , DC test	$R_{\theta JC}$	2	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

**DC Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$ ; $I_{DS} = 100\mu\text{A}$	$V_{DSS}$	65			V
Zero Gate Voltage Drain Leakage Current	$V_{DS} = 28\text{V}$ , $V_{GS} = 0\text{V}$	$I_{DSS}$			1	$\mu\text{A}$
Gate--Source Leakage Current	$V_{GS} = 9\text{V}$ , $V_{DS} = 0\text{V}$	$I_{GSS}$			1	$\mu\text{A}$
Gate Threshold Voltage	$V_{DS} = 28\text{V}$ , $I_D = 300\mu\text{A}$	$V_{GS(th)}$		1.75		V
Gate Quiescent Voltage	$V_{DS} = 28\text{V}$ , $I_{DS} = 150\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		2.7		V

**Pulse CW Signal performance (In Innogrator Test Fixture, 50 ohm system):**  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 140\text{mA}$ ,  $f = 3600\text{MHz}$ , Pulse CW, Pulse Width = 20us, Duty Cycle = 10%.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	$G_p$		16.3		dB
Drain Efficiency@P3dB	$\eta_D$		44.4		%
3dB Compression Point	$P_{-3dB}$		43.3		dBm
Input Return Loss	IRL		-7		dB

**Load Mismatch (In Innogrator Test Fixture, 50 ohm system):**  $V_{DD} = 28\text{Vdc}$ ,  $I_{DQ} = 140\text{mA}$ ,  $f = 3600\text{MHz}$

VSWR 10:1 at 20W Pulsed CW Output Power	No Device Degradation
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### TYPICAL CHARACTERISTICS

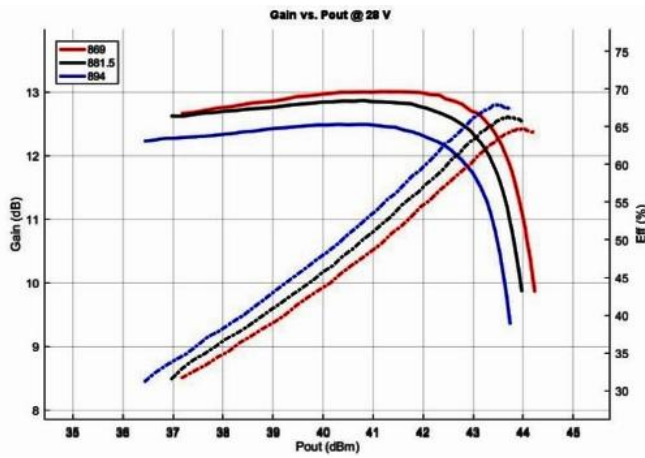


Figure 1. Power gain and drain efficiency as function of Pulse output power (869-894MHz)

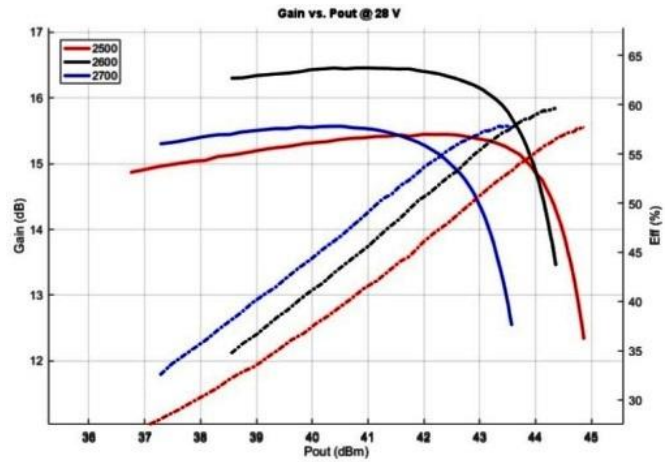


Figure 2. Power gain and drain efficiency as function of Pulse output power (2500-2700MHz)

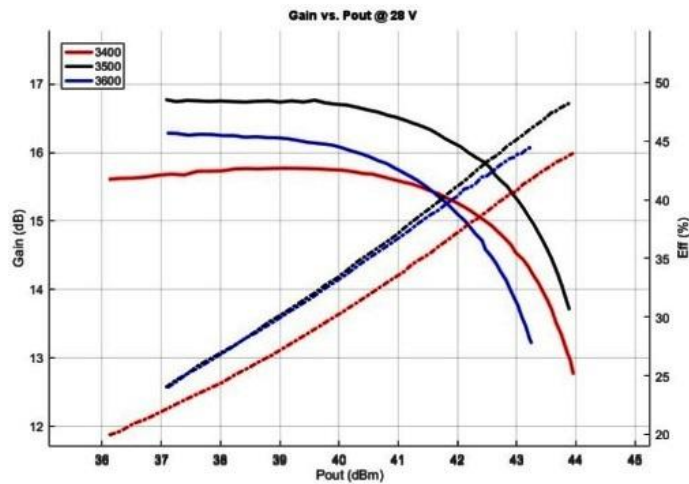
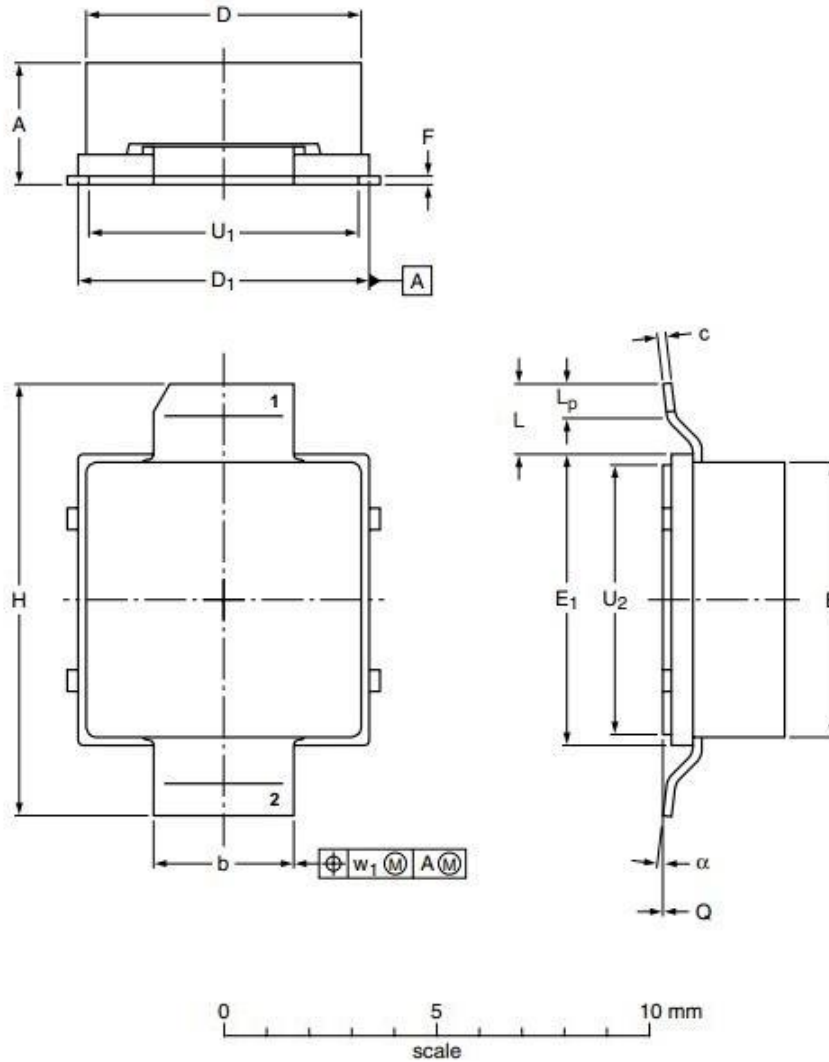


Figure 3. Power gain and drain efficiency as function of Pulse output power (3400-3600MHz)



## Package Outline

Earless Flanged ceramic package; 2 leads



UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	L <sub>p</sub>	Q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	α
mm	3.38	3.38	0.23	6.55	6.93	6.55	6.93	0.23	10.29	1.65	1.02	+0.05	6.43	6.43	0.51	7°
	2.77	3.23	0.18	6.40	6.78	6.40	6.78	0.18	10.03							
inches	0.133	0.133	0.009	0.258	0.273	0.258	0.273	0.009	0.405	0.065	0.040	+0.002	0.253	0.253	0.02	7°
	0.109	0.127	0.007	0.252	0.267	0.252	0.267	0.007	0.395							

OUTLINE VERSION	REFERENCE				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PKG-E-A						10/22/2013



## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/01/22	Rev 1.0	Preliminary Datasheet
2017/08/31	Rev 1.1	Preliminary Datasheet
		Add test data and graph

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