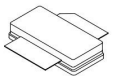
3400-3600MHz, 110W, 28V RF LDMOS FETs

ITCH36110B2



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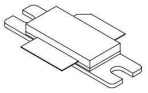


Description

The ITCH36110B2 is a 110-watt, internally-matched LDMOS FETs, designed for cellular application with frequencies from 3400 to 3600MHz. It can biased at class AB or Class C for linear or pulse application as well

•Typical Performance of Demo (On Innogration fixture with device soldered):

V_{DD} =28 Volts, I_{DQ}=**500** mA, Pulse Width=20 us, Duty cycle=10% .

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
3400	50.45	110.9	44.6	11.37	51.21	132.1	44.9
3500	50.41	110.0	44.2	11.56	51.26	133.8	45.1
3600	49.74	94.1	41.7	11.05	50.6	114.7	42.6

Typical Single-Carrier W-CDMA Performance (On Test Fixture with device soldered):

V_{DD}=28Volts, I_{DQ} = **800** mA, WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz, PAR =10.5 dB at 0.01 % probability on CCDF.

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Eff (%)
3400	39	10.53	-41.8	12.4	14.0
3500	39	10.62	-38.9	12.6	13.7
3600	39	10.30	-40.8	12.1	14.0
3400	40	10.11	-41.3	12.4	15.9
3500	40	10.31	-38.6	12.6	15.6
3600	40	9.98	-39.8	12.2	15.9

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 300 μA)	$V_{GS(th)}$		2.2		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 550 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.6	3.5	V

Functional Tests (In Innogration Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f =3500 MHz, Pulsed CW Signal Measurements.

Pulse width: 20uS,duty cycle: 10%

Power Gain	G_p		10		dB
3 dB Compression Point	P_{3dB}		110		W
Drain Efficiency@P3dB	η_D		45		%
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f = 3500 MHz

VSWR 10:1 at 10W WCDMA Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

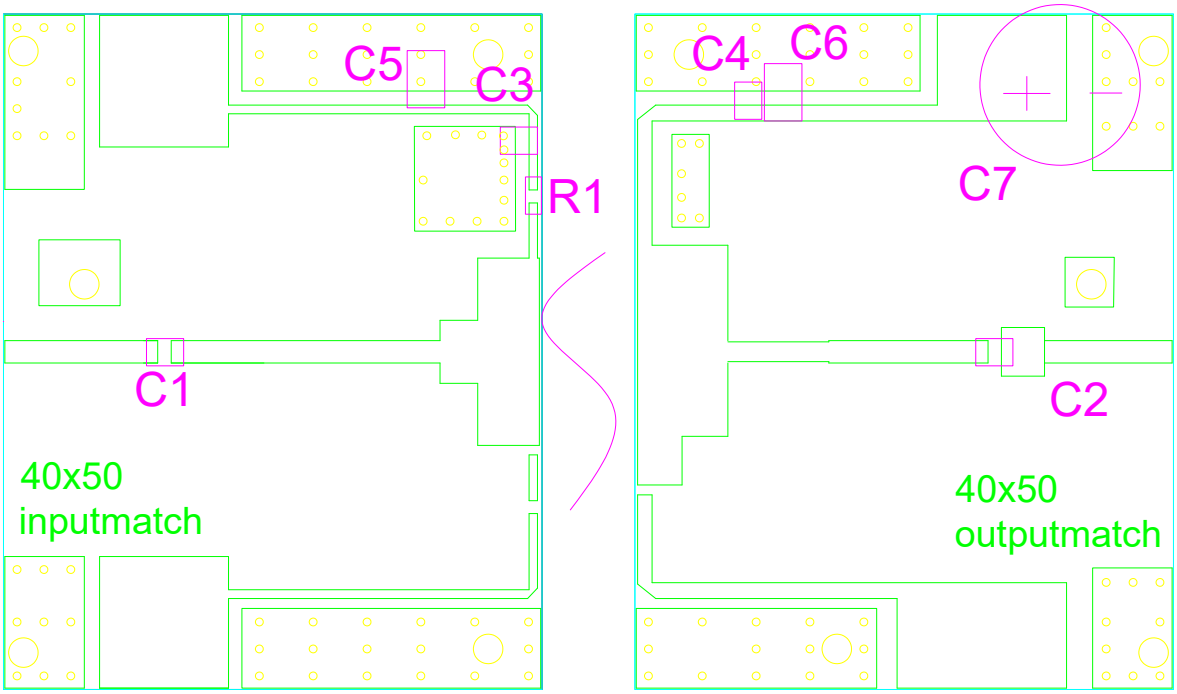


Figure 1. Test Circuit Component Layout （PCB RO4350B 20mils）

Table 5. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C2, C3, C4	0805	8.2pF	4
C5, C6	1210	10uF/100V	2
C7		220uF/63V	1
R1	0603	10R	1

TYPICAL CHARACTERISTICS

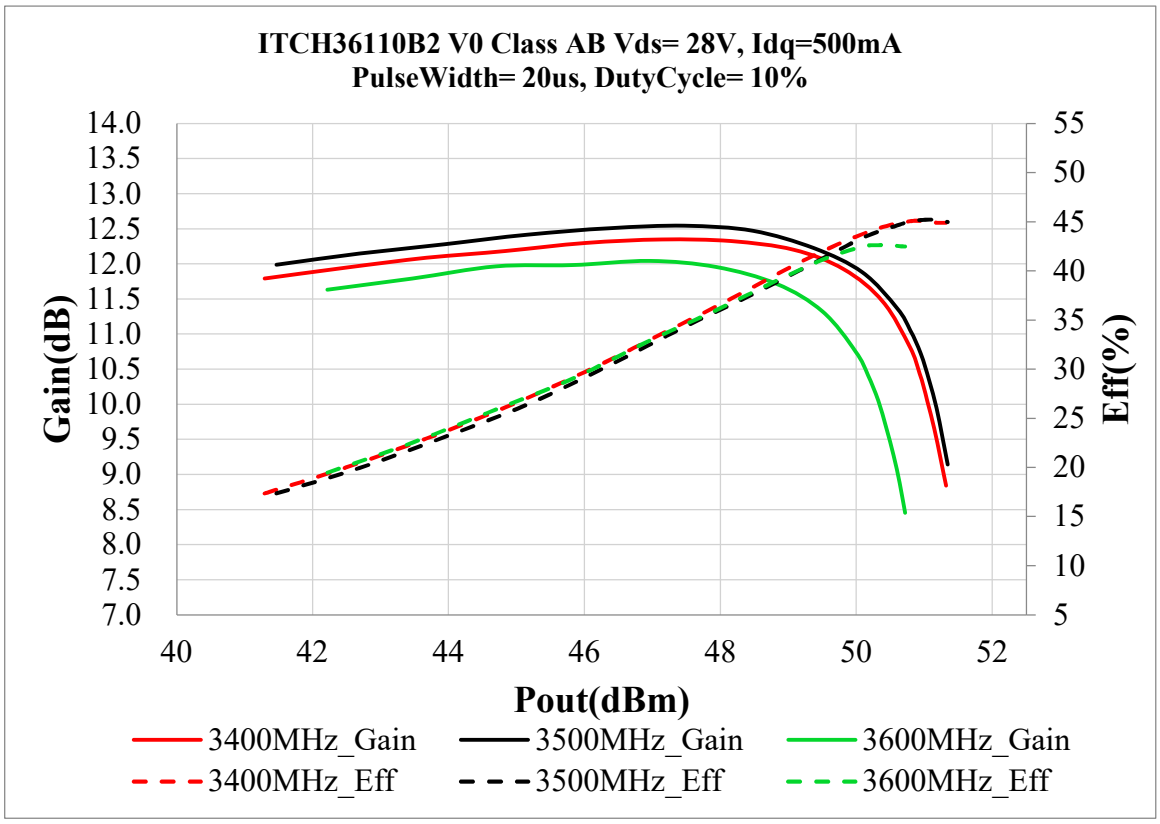


Figure 2. Power gain and drain efficiency as function of pulsed CW Pout

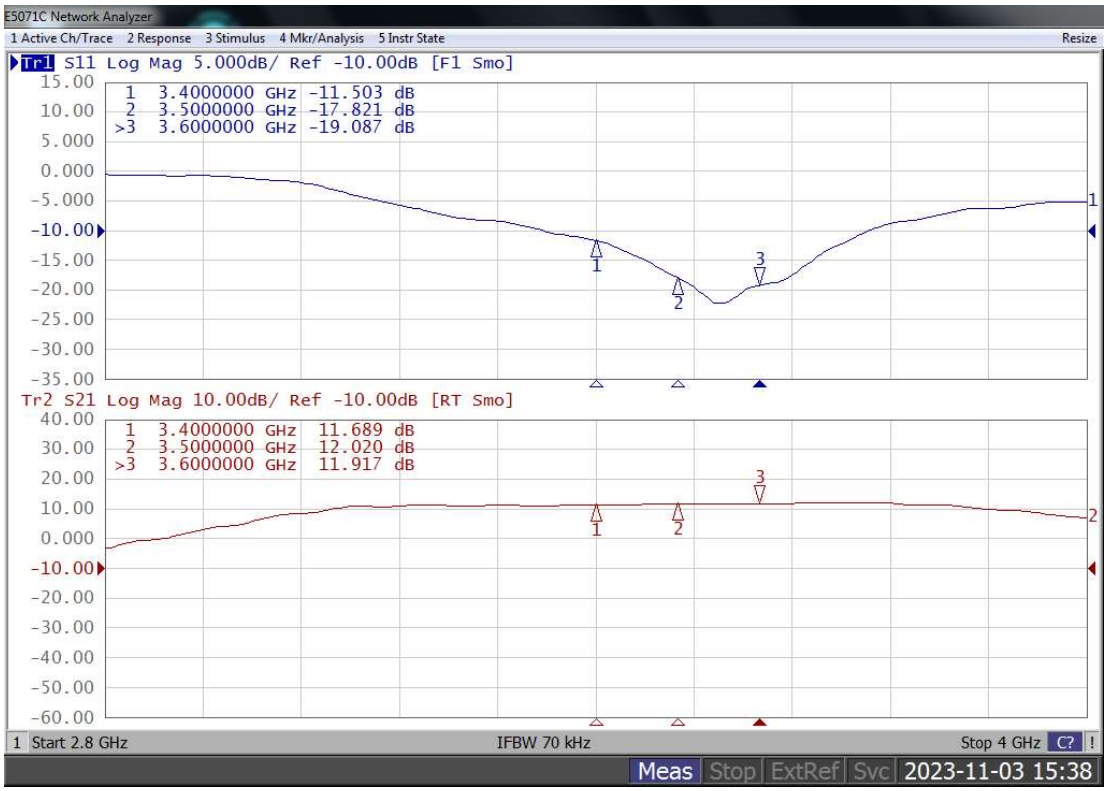
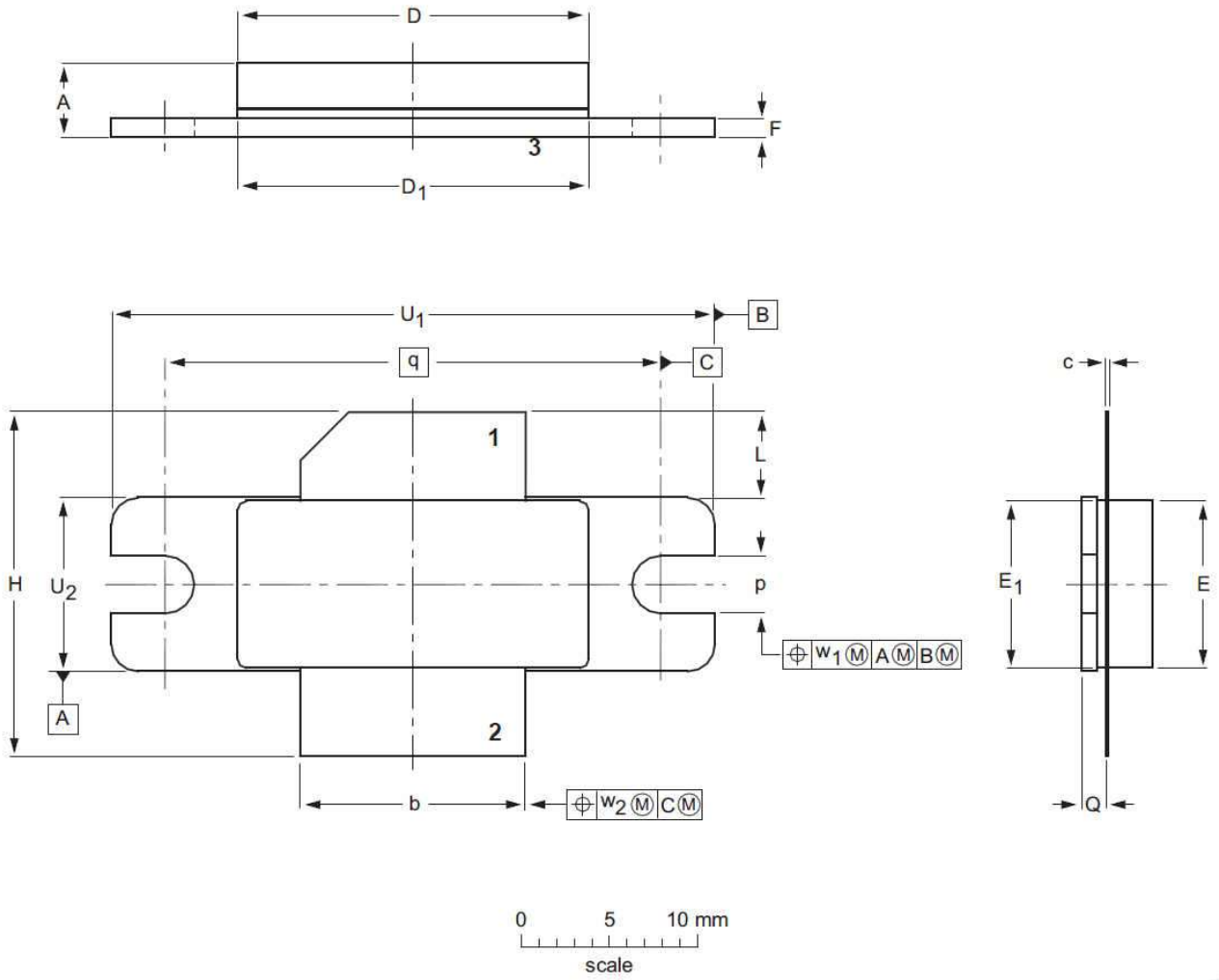


Figure 3. Broadband Frequency Response

Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

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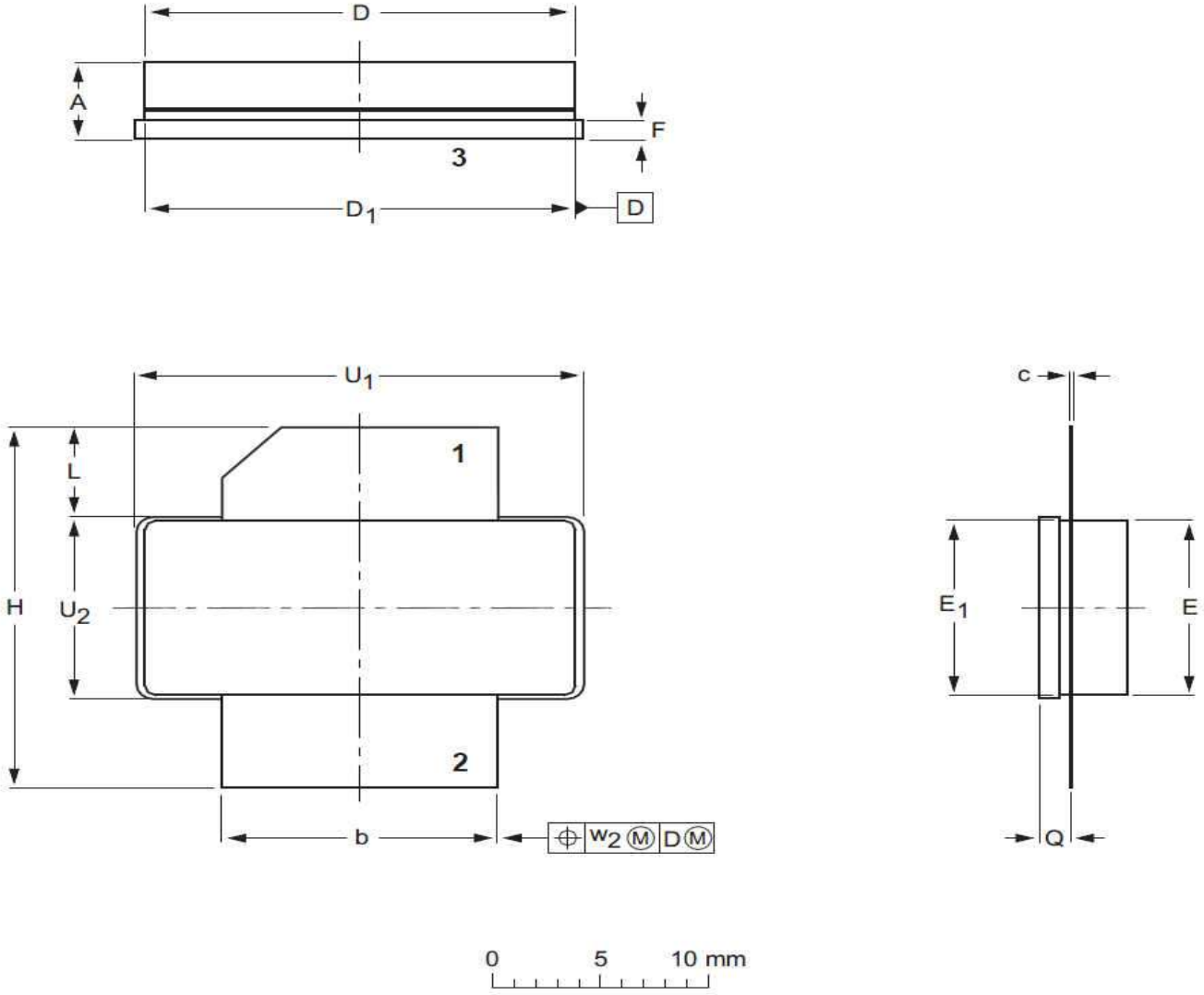
PKG-B2E					03/12/2013

Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/11/3	Rev 1.0	Preliminary Datasheet Creation

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