



2500MHz-2700MHz, 150W, 28V High Power RF LDMOS FETs

Description

The ITCH27150C2 is a 150-watt, internally matched LDMOS FET, designed for multicarrier WCDMA/PCS/DCS/LTE base station and ISM applications with frequencies from 2500 to 2700 MHz. It Can be used in Class AB/B and Class C for all typical cellular base station modulation formats.



•Typical Performance (On Innegration fixture with device soldered):

VDD = 28 Volts, I_{DQ} = 1000 mA, Pulse CW, Pulse Width=100 us, Duty cycle=10% .

Frequency	G _p (dB)	P _{-1dB} (dBm)	η _D @P ₋₁ (%)	P _{-3dB} (dBm)	η _D @P ₋₃ (%)
2500 MHz	14.7	51.9	47.4	52.6	47.6
2600 MHz	14.9	52.2	47.5	52.9	48.3
2700 MHz	14.8	51.6	50.5	52.3	50.1

•Typical Performance (On Test Fixture with device soldered):

V_{DD}=28Volts, I_{DQ} = 50 mA, CW.

Frequency	P _{OUT} (W)	G _p (dB)	η _D (%)
2500 MHz	170	11.7	52.1
2600 MHz	170	11.0	55.1
2700 MHz	170	10.4	58.6

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	70	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _C = 85°C, T _J =200°C, DC test	R _{θJC}	0.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class



Human Body Model (per JESD22--A114)	Class 2
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Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =1mA)	V _{DSS}	65	70		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{DSS}			10	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}			1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 600 uA)	V _{GS(th)}		1.8		V
Gate Quiescent Voltage (V _{DD} = 28 V, I _{DQ} = 1000 mA, Measured in Functional Test)	V _{GS(Q)}	2.3	2.8	3.3	V

Functional Tests (On Innogrations demo, 50 ohm system) : V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 2700 MHz, Pulse CW, Pulse Width=20 us, Duty cycle=10% .

Power Gain (Maximum Gain)	G _p		14.8		dB
1 dB Compression Point	P _{-1dB}		51.6		dBm
3dB Compression Point	P _{-3dB}		52.3		dBm
Drain Efficiency@P3dB	η _D		50.1		%
Input Return Loss	IRL		-7		dB

Load Mismatch (On Innogrations Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 2700 MHz

VSWR 10:1 at 150W pulse CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram

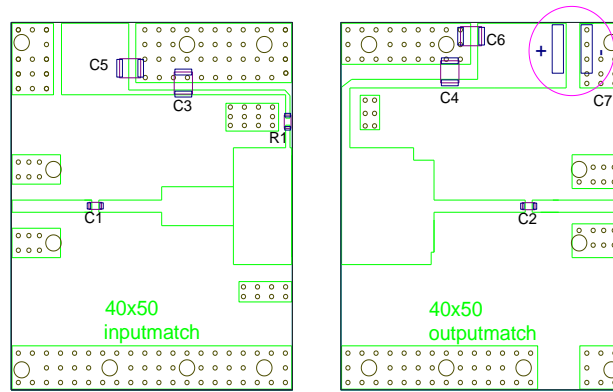


Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer	P/N
C1,C2	Ceramic Capacitor,8.2pF	ATC	600F
C3,C4	Ceramic Capacitor,8.2pF	ATC	800B
C5,C6	10uF 100V chip Capacitor		
C7	Electrolytic Capacitor ,100uF,50V		
R1	Chip Resistor,10 Ω		
PCB	0.762mm [0.030"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper		

TYPICAL CHARACTERISTICS

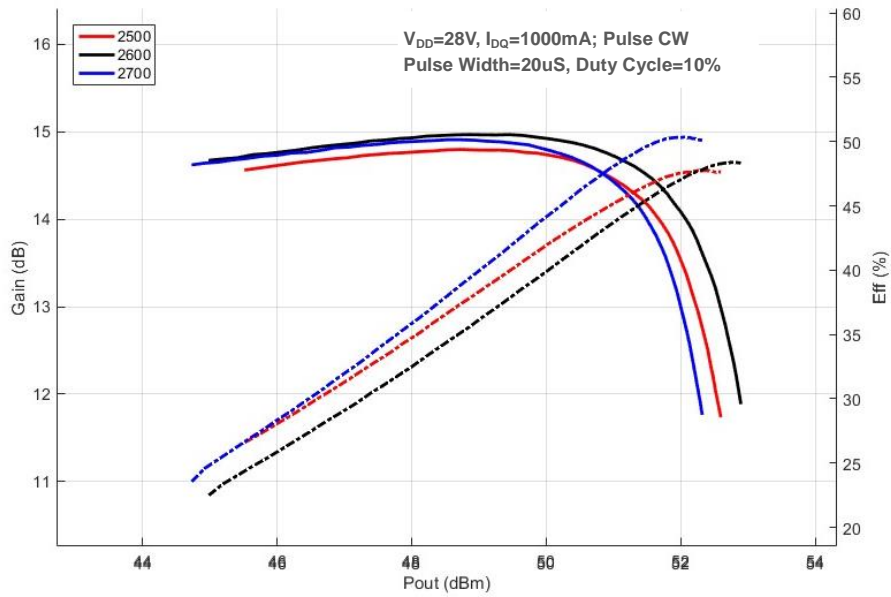


Figure 2. Power gain and drain efficiency as function of Pulse output power (2500MHz-2700MHz)

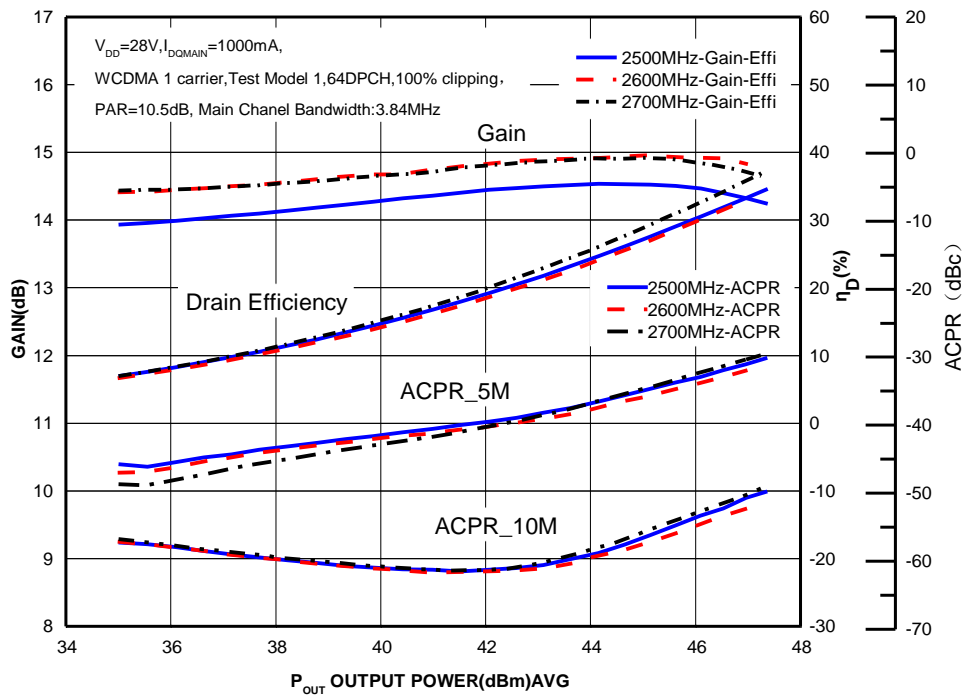
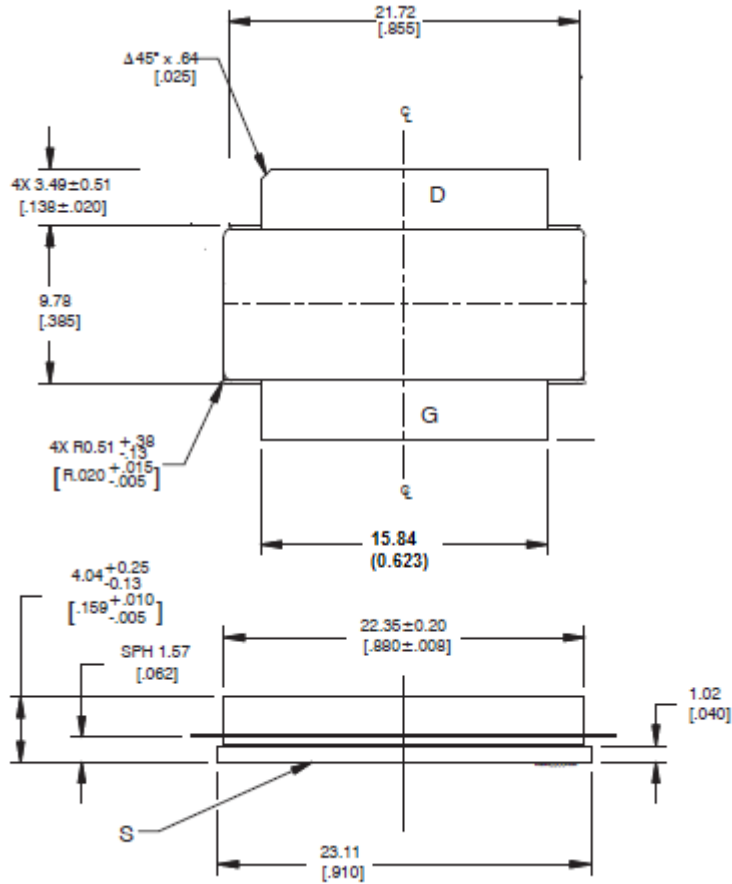


Figure 3. Single-Carrier WCDMA Power Gain and Drain Efficiency and ACPR at 5 MHz and at 10 MHz as Function of Average Output Power



Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2018/12/04	Rev 1.0	Preliminary Datasheet

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