Innogration (Suzhou) Co., Ltd.

Document Number: GTAH58045GX
Preliminary Datasheet V1.0

Gallium Nitride 28V 45W, RF Power Transistor

Description

GTAH58045GX

The GTAH58045GX is a 45W internally matched, GaN HEMT, designed for multiple applications, especially sub-6GHz LTE/LTE-A/LTE-U from 4400-5900MHz.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical **pulsed** performance (on 5.7-5.9GHz fixture with device soldered)

V_{DD}=28V I_{DQ}=130mA, Pulse CW, Pulse width=20uS, Duty cycle=10%.

Freq(MHz)	P1(dBm)	P3(dBm)	P3(W)	Eff(%)@P3	Gain @P1 (dB)
5700	46.76	48.03	63.6	53.43	12.95
5800	46.23	47.62	57.8	53.84	13.46
5900	45.69	47.02	50.4	54.32	13.38

- Typical **CW** performance (on 5.7-5.9GHz fixture with device soldered)

  V_{DD}=28V I_{DQ}=130mA

Freq(MHz)	Pin (dBm)	Psat(W)	Ids（A）	Eff(%)
5700	37.1	60.0	4.24	50.54
5800	36.6	54.1	3.82	50.58
5900	36.6	48.5	3.42	50.65

- Typical **modulation** performance (on 5.7-5.9GHz fixture with device soldered)

  V_{DD}=28V, I_{DQ}=130mA, 1 carrier WCDMA signal, (PAR=10.5dB @ 0.01% probability).

Freq(MHz)	Pout(dBm)	ACPR(dBc)	Gain(dB)	Eff(%)
5700	39.2	-36.5	13.29	24.56
5800	39.2	-37.8	13.95	25.76
5900	39.2	-36.3	13.79	28.33

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC
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Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (28V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	150	Vdc
Gate--Source Voltage	V_{GS}	-10,+2	Vdc

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Operating Voltage	V_{DD}	40	Vdc
Maximum Forward Gate Current @ Tc = 25°C	Igmax	12	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature(See note 1)	T_J	+200	°C
Total Device Power Dissipation (Derated above 25°C, see note 2)	Pdiss	86	W

Note: 1. Continuous operation at maximum junction temperature will affect MTTF
2.Bias Conditions should also satisfy the following expression: Pdiss < (Tj – Tc) / RJC and Tc = Tcase

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, RF CW operation	RθJC	2.3	C/W

Table 3. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

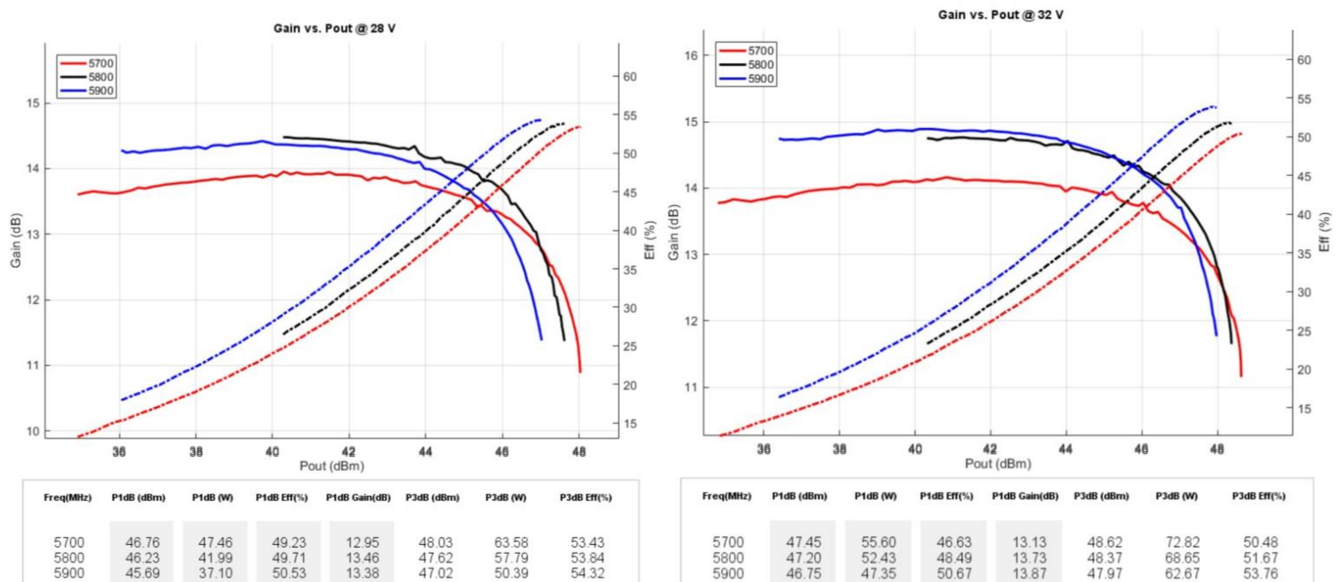
DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=12mA	V_{DSS}	150			V
Gate Threshold Voltage	V_{DS} = 28V, I_D =12mA	V_{GS}(th)		-2.7		V
Gate Quiescent Voltage	V_{DS} =28V, I_{DS}=130mA, Measured in Functional Test	$V_{GS(Q)}$		-2.33		V

Functional Tests (In 5.7-5.9GHz wideband Production Test Fixture, 50 ohm system) :V_{DD} = 28 Vdc, I_{DQ} = 130 mA, f = 5800 MHz, WCDMA signal, Pout=9W

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	Gp		13		dB
Drain Efficiency @ P_{out}	Eff		25		%
Saturated Power by CCDF test	P_{SAT}	45			W
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases (Device no damage)	VSWR		10:1		Ψ

Figure 1: Pulsed CW performance at 28V(Left) and 32V(Right)

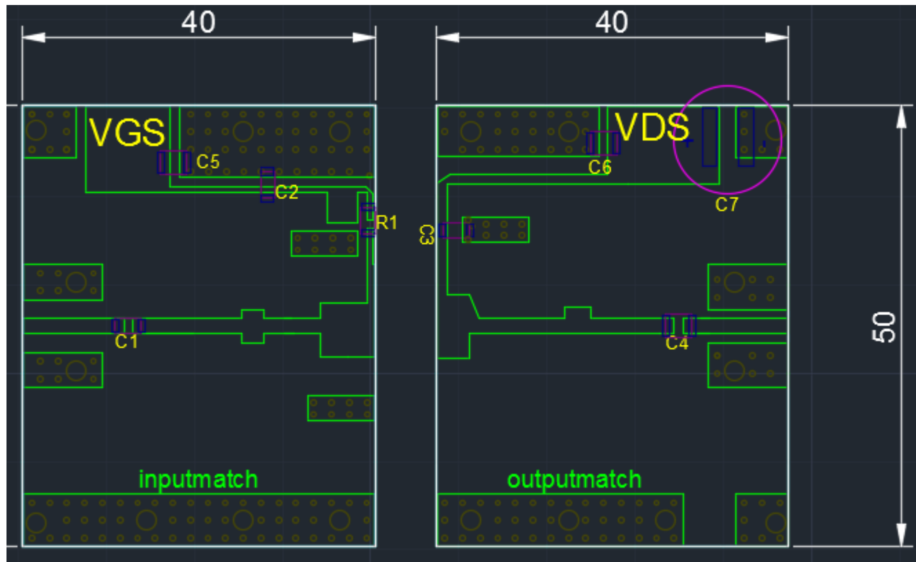


Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
5700	46.76	47.46	49.23	12.95	48.03	63.58	53.43
5800	46.23	41.99	49.71	13.46	47.62	57.79	53.84
5900	45.69	37.10	50.53	13.38	47.02	50.39	54.32

Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
5700	47.45	55.60	46.63	13.13	48.62	72.82	50.48
5800	47.20	52.43	48.49	13.73	48.37	68.65	51.67
5900	46.75	47.35	50.67	13.87	47.97	62.67	53.76

Figure 2: Photo of 5.7-5.9GHz application circuit

PCB:RO4350 30Mil (Layout gerber file upon request) unit:mm



C1,C2 ,	5.6pF
C3,C4	3.3pF
C5, C6	10uF
C7	220uF,100V
R1	10ohm

Package Outline

Flanged ceramic package; 2 leads

Pin Connection		
1	2	3
Drain	Gate	Source

Unit: mm
Tolerances(unless specified): x.x ±0.1
x.xx ±0.05

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

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Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2017/12/13	V1.0	Preliminary Datasheet Creation

Notice

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