MR2006C LDMOS TRANSISTOR

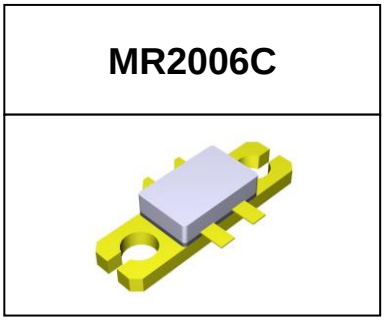
Document Number: MR2006C
Objective Datasheet V1.1

24W, 12.5V High Power RF LDMOS FETs

Description

The MR2006C is a 24-watt, Push-Pull configuration, unmatched LDMOS FETs, designed for ISM and Mobile radio applications with frequencies under 2GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

It can also operate at 13.6V, 14V etc with increased power capability.



- Typical Performance (On Innogration fixture with device soldered):
  V_{DD} = 12.5 Volts, I_{DQ} = 200 mA, CW.

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
100	28.5	43.7	23.4	2.81	15.2	66.7%
150	26.4	43.6	22.9	2.71	17.2	67.6%
200	27.9	44	25.1	2.92	16.1	68.8%
250	26.8	43.6	22.9	2.69	16.8	68.1%
300	25.3	43.3	21.4	2.36	18	72.5%
350	25.9	43.1	20.4	2.3	17.2	71.0%
400	26.3	43	20.0	2.4	16.7	66.5%
450	25.4	42.9	19.5	2.35	17.5	66.4%
500	26	42.9	19.5	2.33	16.9	66.9%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- HF Amplifier
- UHF Amplifier
- Vehicle radio
- VHF Amplifier
- Wideband Amplifier
- Beidou Navigation

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	65	69		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS(th)}$	——	1.95	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =14 V, f = 1 MHz)	C_{ISS}		24.8		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =14 V, f = 1 MHz)	C_{OSS}		14.0		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =14 V, f = 1 MHz)	C_{RSS}		0.65		pF
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		24.6		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		10.6		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		0.53		pF

Functional Tests (On Demo Test Fixture, 50 ohm system) V_{DD} = 12.5 Vdc, I_{DQ} = 200 mA, f = 500 MHz, CW Signal Measurements, Pin=26dBm

Power Gain	Gp		16.9		dB
Drain Efficiency@Pout	η_D		66		%
Output Power	P_{out}		19.5		W
Input Return Loss	IRL		-7		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 12.5Vdc, I_{DQ} = 200 mA, f = 500 MHz

VSWR 10:1 at 19.5W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: Power gain and drain efficiency as function of Pulse output power

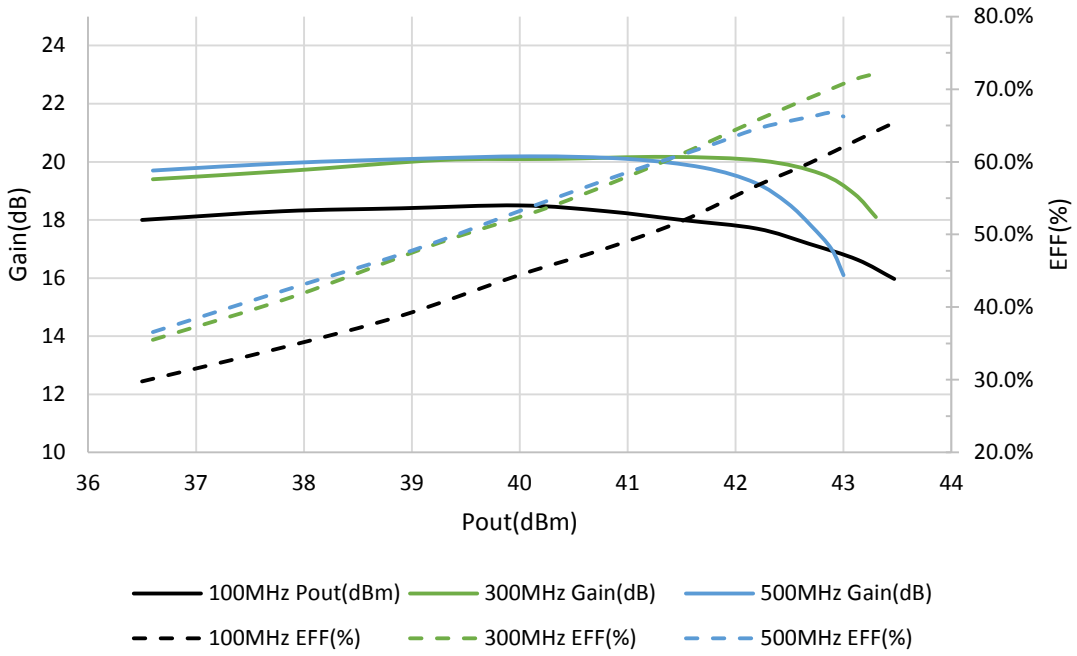
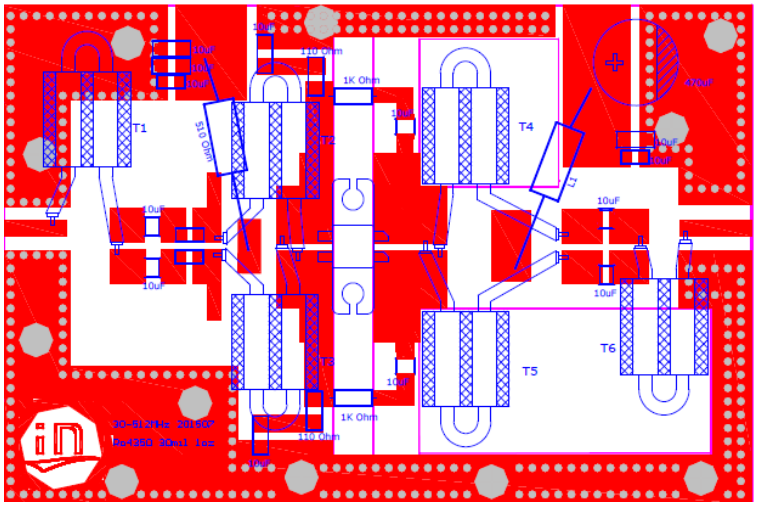
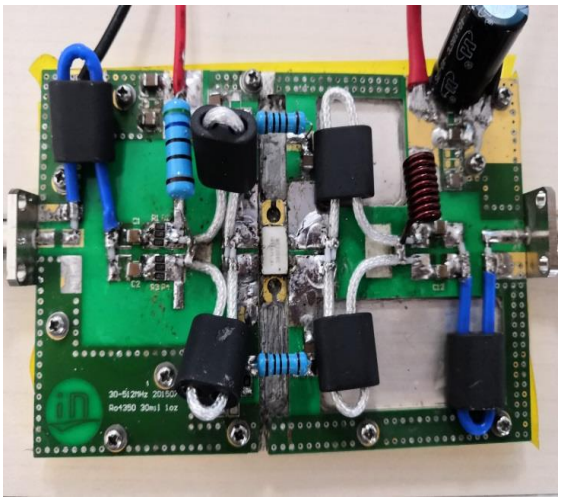


Figure 2: 108-512MHz wideband application circuit picture

(PCB Materials: Roger 4350B, 30Mil, Layout file upon request)

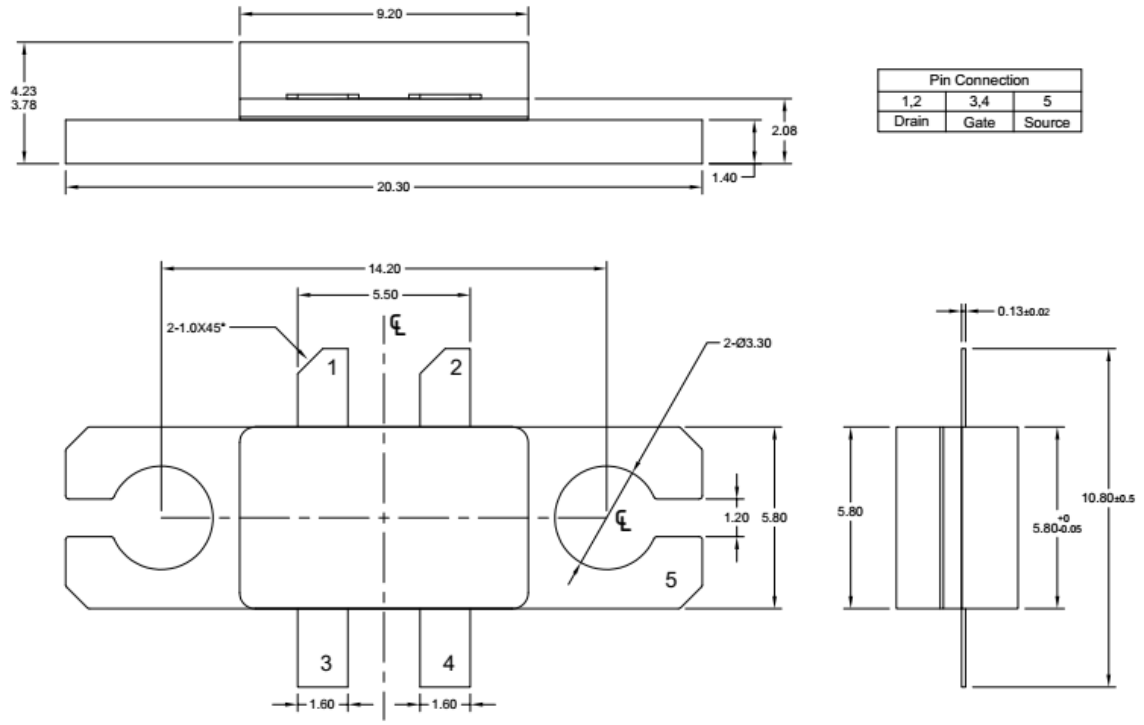




BOM	
L1	6uH 5A air core inductance
T1，T6	magnetic core: BN-61-102 RF cable: SF-086-50, 70mm length
T2，T3， T4，T5	magnetic core: BN-61-102 RF cable: SFF-25-1.5, 70mm length

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-G4E					2018/01/19

Figure 1. Package Outline PKG-G4E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/6/14	Rev 1.0	Objective Datasheet
2018/9/16	Rev 1.1	Preliminary Datasheet

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