

MR2003C LDMOS TRANSISTOR

Document Number: MR2003C
Preliminary Datasheet V1.1

18W, 12.5V High Power RF LDMOS FETs

Description

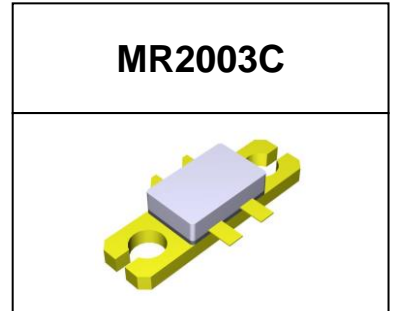
The MR2003C is a 18-watt, Push-Pull configuration, unmatched LDMOS FETs, designed for ISM and Mobile radio applications with frequencies under 2GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

It can also operate at 13.6V, 14V etc with increased power capability.

- Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 12.5$ Volts, $I_{DQ} = 150$ mA, CW.

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
100	28	42.4	17.4	2.34	14.4	59.4%
150	26.8	42.5	17.8	2.4	15.7	59.3%
200	26.9	42.4	17.4	2.38	15.5	58.4%
250	28.8	42.8	19.1	2.45	14	62.2%
300	27.2	42.5	17.8	2.15	15.3	66.2%
350	25.4	42	15.8	1.89	16.6	67.1%
400	26.6	41.9	15.5	1.86	15.3	66.6%
450	28.3	42.4	17.4	2.31	14.1	60.2%
500	27.8	42.3	17.0	2.24	14.5	60.7%
550	27.7	42	15.8	2.12	14.3	59.8%



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- HF Amplifier
- UHF Amplifier
- Vehicle radio
- VHF Amplifier
- Wideband Amplifier
- Beidou Navigation

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
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Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 1.0\text{mA}$	$V_{(BR)DSS}$	65	70		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	---	---	1	μA
Gate--Source Leakage Current ($V_{GS} = 9\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	---	2.17	---	V
Common Source Input Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 14\text{V}$, $f = 1\text{MHz}$)	C_{ISS}		15.7		pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 14\text{V}$, $f = 1\text{MHz}$)	C_{OSS}		6.0		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 14\text{V}$, $f = 1\text{MHz}$)	C_{RSS}		0.42		pF
Common Source Input Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{ISS}		16.0		pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{OSS}		4.6		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{RSS}		0.38		pF

Functional Tests (On Demo Test Fixture, 50 ohm system) $V_{DD} = 12.5\text{Vdc}$, $I_{DQ} = 150\text{mA}$, $f = 500\text{MHz}$, CW Signal Measurements,
 $P_{in} = 27.8\text{dBm}$

Power Gain	G_p		14.5		dB
Drain Efficiency@Pout	η_D		60		%
Output Power	P_{out}		17		W
Input Return Loss	IRL		-5		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 12.5\text{Vdc}$, $I_{DQ} = 150\text{mA}$, $f = 500\text{MHz}$

VSWR 10:1 at 18W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 1: Power gain and drain efficiency as function of Pulse output power

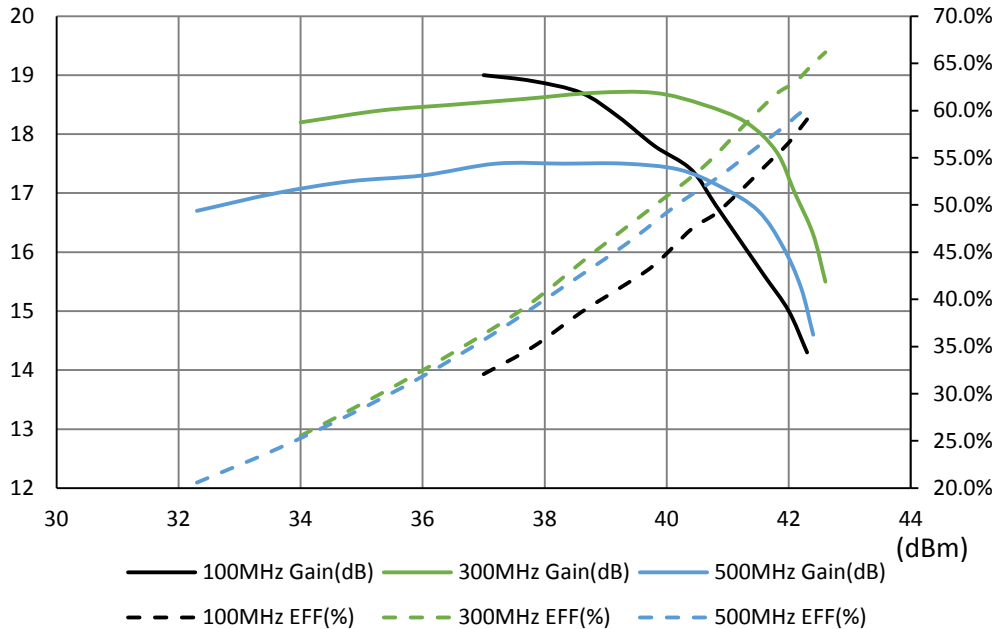
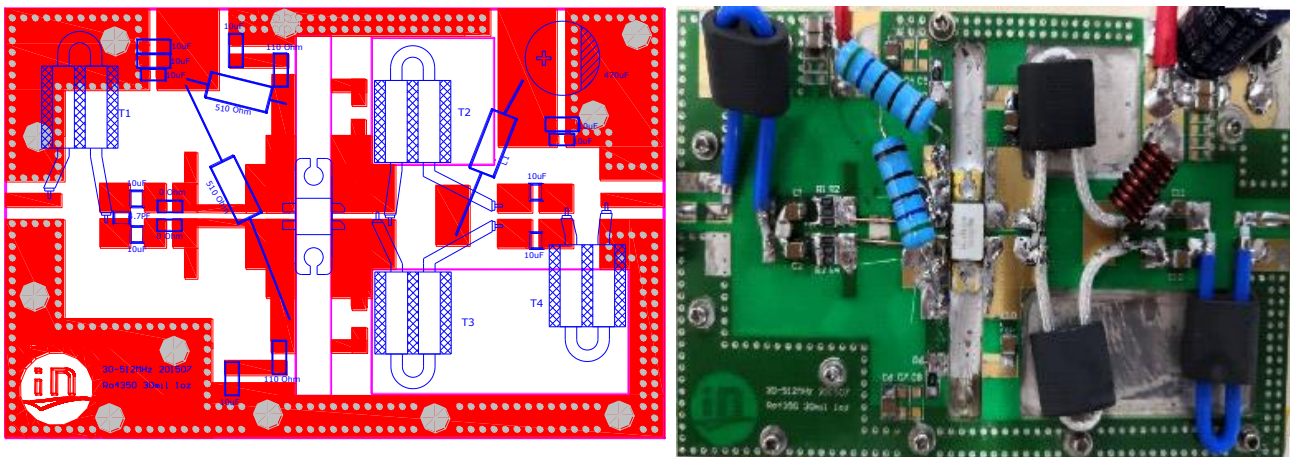


Figure 2: 108-512MHz wideband application circuit picture
(PCB Materials: Roger 4350B, 30Mil, Layout file upon request)



BOM	
L1	6uH 5A air core inductance
T1, T4	magnetic core: BN-61-102 RF cable: SF-086-50, 70mm length
T2, T3	magnetic core: BN-61-102 RF cable: SFF-25-1.5, 70mm length

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads

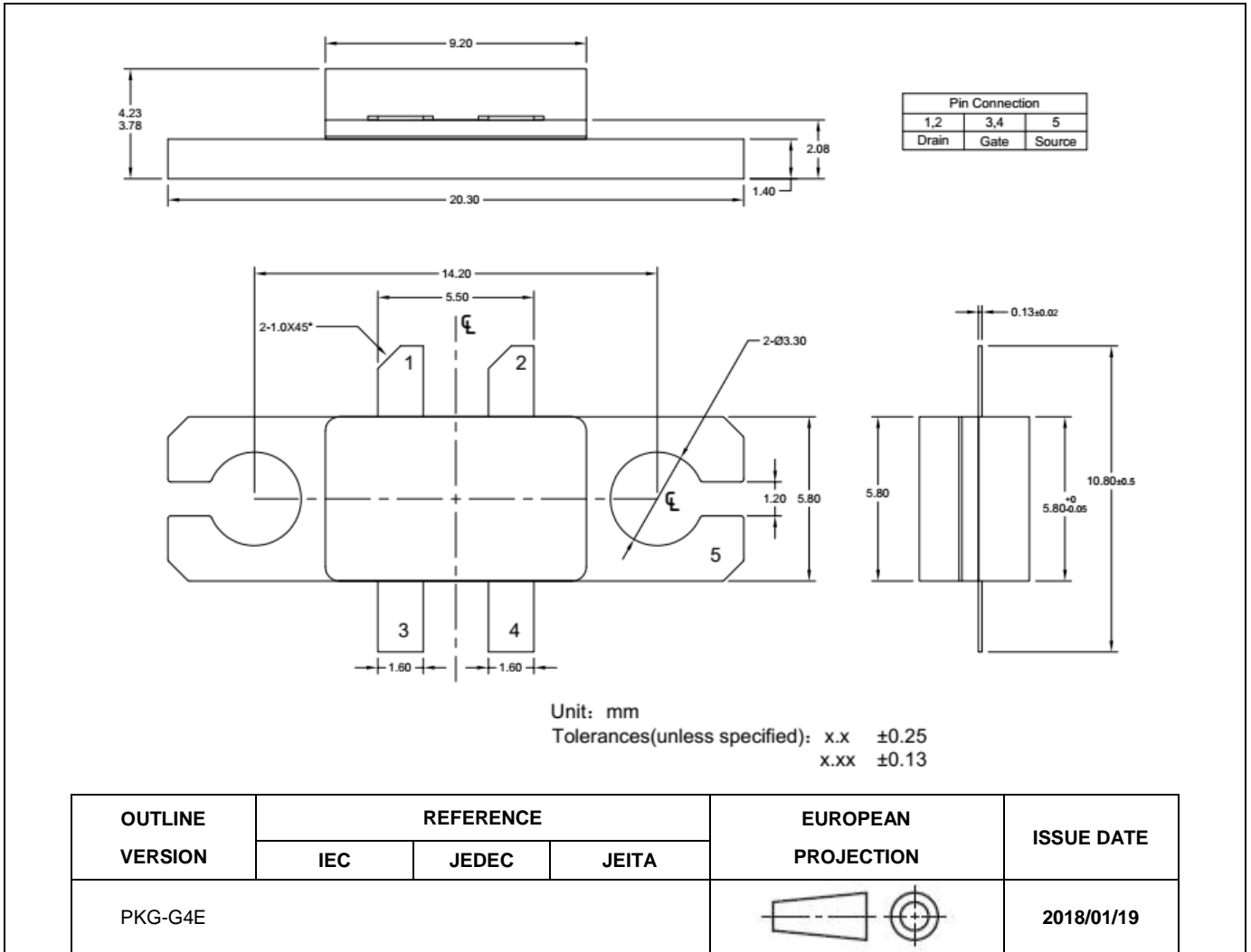


Figure 1. Package Outline PKG-G4E

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/6/14	Rev 1.0	Preliminary Datasheet
2018/9/16	Rev 1.1	12.5V data added

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