

MM2001V LDMOS TRANSISTOR

Document Number: MM2001V
Preliminary Datasheet V1.0

10W, 50V High Power RF LDMOS FETs

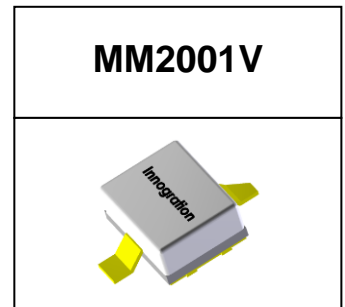
Description

The MM2001V is a 10-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies up to 2 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

- Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 48\text{ V}$, $I_{DQ} = 10\text{ mA}$, Pulse CW, Pulse Width=10uS, Duty Cycle=10%.

Freq(MHz)	P_{1dB} (dBm)	$G_P @ P_{1dB}$ (dB)	P_{3dB} (dBm)	$\eta_D @ P_{3dB}$ (%)
960	43.7	15.3	44.4	55.3
1000	43.8	15.6	44.5	56.6
1050	44.3	15.5	44.8	58.2
1100	44.4	16.4	44.8	59.3
1150	44.2	16.4	44.7	59.6
1200	44.1	16.9	44.5	60.4
1250	43.9	16.7	44.3	60.3
1300	43.6	16.8	44.2	60.5
1350	43.4	16.6	44.0	61.0
1400	43.2	16.0	43.8	59.6



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCl drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 960-1215MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

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Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C=85^\circ\text{C}$, $T_J=200^\circ\text{C}$, DC test	$R_{\theta JC}$	3	$^\circ\text{C/W}$

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Voltage $V_{GS}=0$, $I_{DS}=1.0\text{mA}$	$V_{(BR)DSS}$		115		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 90\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}$, $I_D = 600\ \mu\text{A}$)	$V_{GS(th)}$	—	2.82	—	V
Gate Quiescent Voltage ($V_{DD} = 48\text{V}$, $I_D = 10\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.0	—	V
Common Source Input Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 40\text{V}$, $f = 1\text{MHz}$)	C_{ISS}		11.4		pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 40\text{V}$, $f = 1\text{MHz}$)	C_{OSS}		4.9		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 40\text{V}$, $f = 1\text{MHz}$)	C_{RSS}		0.05		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 48\text{Vdc}$, $I_{DQ} = 10\text{mA}$, $f = 2000\text{MHz}$

VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram

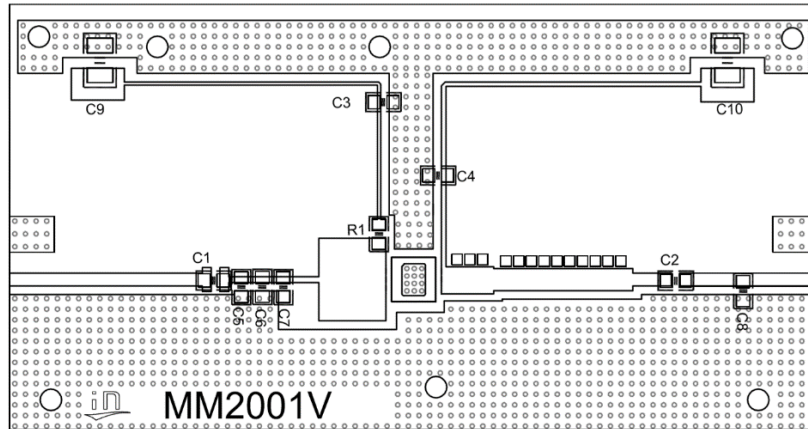


Figure 1. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Part	description	Model
C1,C2,C3,C4	33pF	ATC600F
C5	2pF	ATC600F
C6,C7,C8	1pF	ATC600F
C9,C10	10uF	
R1	10 ohm	
PCB	0.508mm [0.020"] thick, $\epsilon_r=3.48$, Rogers RO4350B, 1 oz. copper	

TYPICAL CHARACTERISTICS

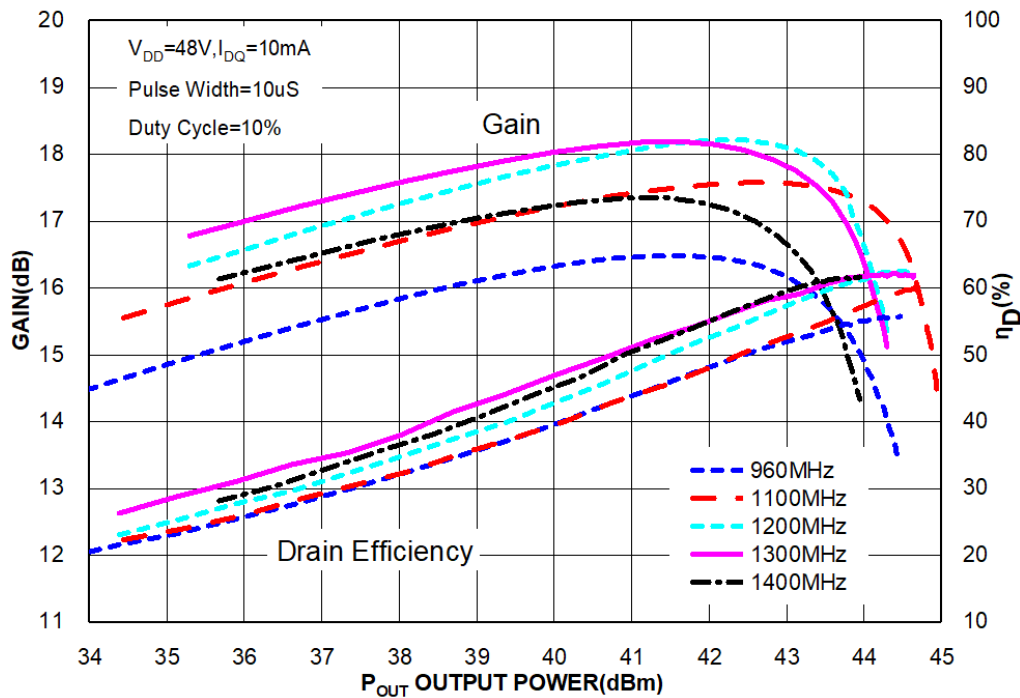


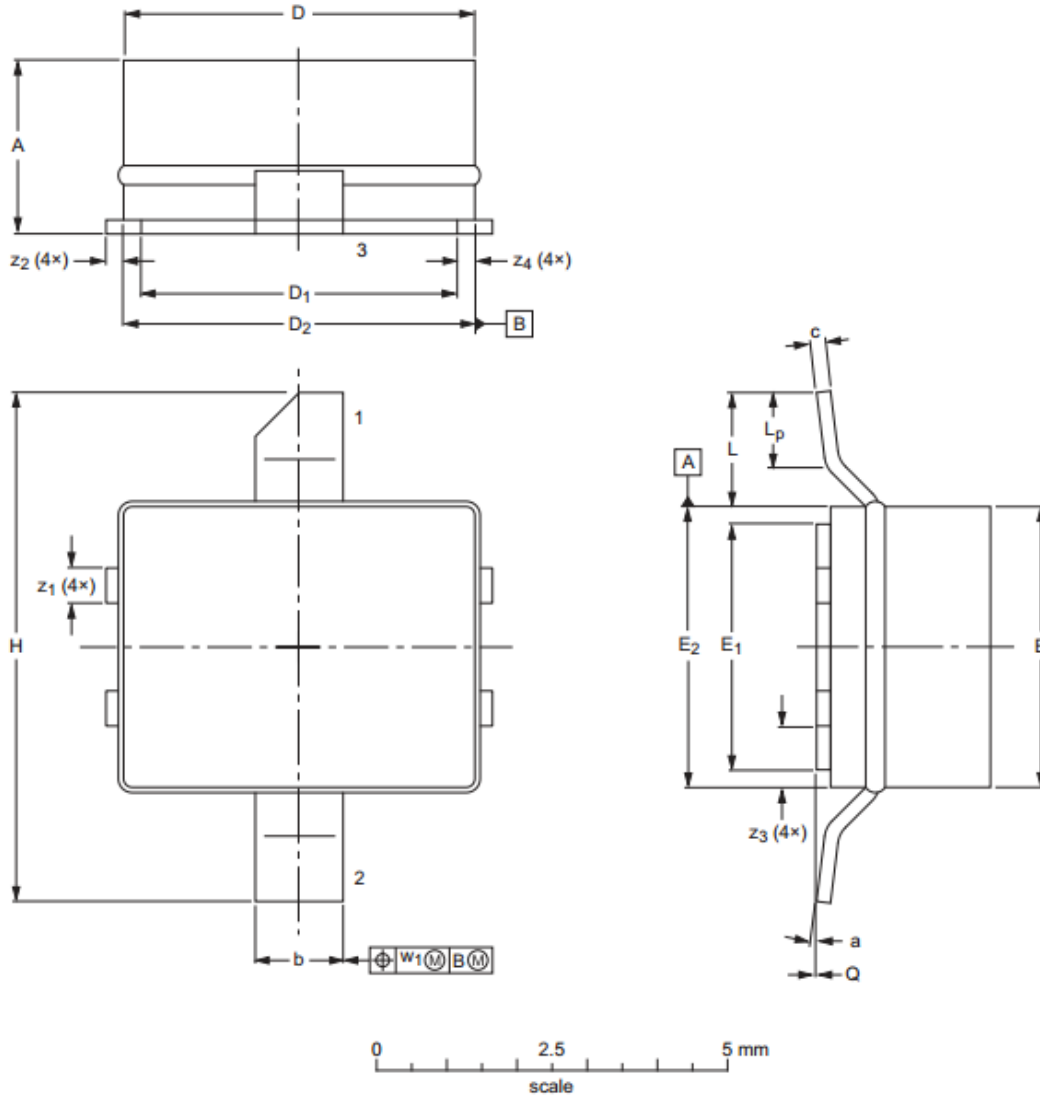
Figure 2. Power Gain and Drain Efficiency as function of Power Out

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Package Outline

Earless Flanged ceramic package; 2 leads(1-Drain,2-Gate,3-Source)



UNIT	A	b	c	D	D ₁	E	E ₁	E ₂	H	L	L _p	Q	w ₁	z ₁	z ₂	z ₃	z ₄	α
mm	2.34	1.35	0.23	5.16	4.65	4.14	3.63	4.14	7.49	2.03	1.02	0.1	0.25	0.58	0.25	0.97	0.51	7°
	2.13	1.19	0.18	5.00	4.50	3.99	3.48	3.99	7.24	1.27	0.51	0.0		0.43	0.18	0.81	0.00	0°

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-MM					18/6/2014

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Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2019/11/18	Rev 1.0	Preliminary Datasheet

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