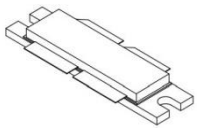
MQ051K1VPX LDMOS TRANSISTOR

Document Number: MQ051K1VPX
Preliminary Datasheet V1.2

1000W, 50V High Power RF LDMOS FETs

MQ051K1VPX



Description

The MQ051K1VPX is a 1000-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 500MHz. It is also featured with high ruggedness as well.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical Performance (On Innogration FM fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 200 mA, CW.

Freq (MHz)	Trade off	Pout(W)	Gain (dB)	Eff (%)
88-108	Power tuned	1120	18	75
88-108	Efficiency tuned	1020	20	79

- Typical Performance (On Innogration narrow band fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 1300 mA, CW.

Freq(MHz)	Pout(dBm)	Gain(dB)	Eff(%)
1.6	56	23.3	52
5	56	22.8	58
10	56	21.5	59
15	56	21.3	59
20	56	22.2	56
25	56	23.4	53
30	56	23	51

- Typical Performance (On Innogration narrow band fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 1300 mA, 2-Tone CW Signal with Spacing 650Hz

Freq(MHz)	Pavg(dBm)	Gain(dB)	Eff(%)	IMD3(dBc)
1.6	53	23.6	40	-34
5	53	22.7	44	-33
10	53	21.6	45	-35
15	53	21.3	45	-36
20	53	22.2	43	-35
25	53	23.4	41	-33
30	53	22.9	39	-32.5

- Typical Performance (On Innogration narrow band fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 100 mA, Pulse CW: Pulse width=200uS, Duty Cycle=20%.

Freq(MHz)	P_{SAT}(W)	G_P(dB)	Eff(%)
27	1072	24.5	70

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 1000W CW, 50 Vdc, I_{DQ} = 100 mA	$R_{\theta JC}$	0.15	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

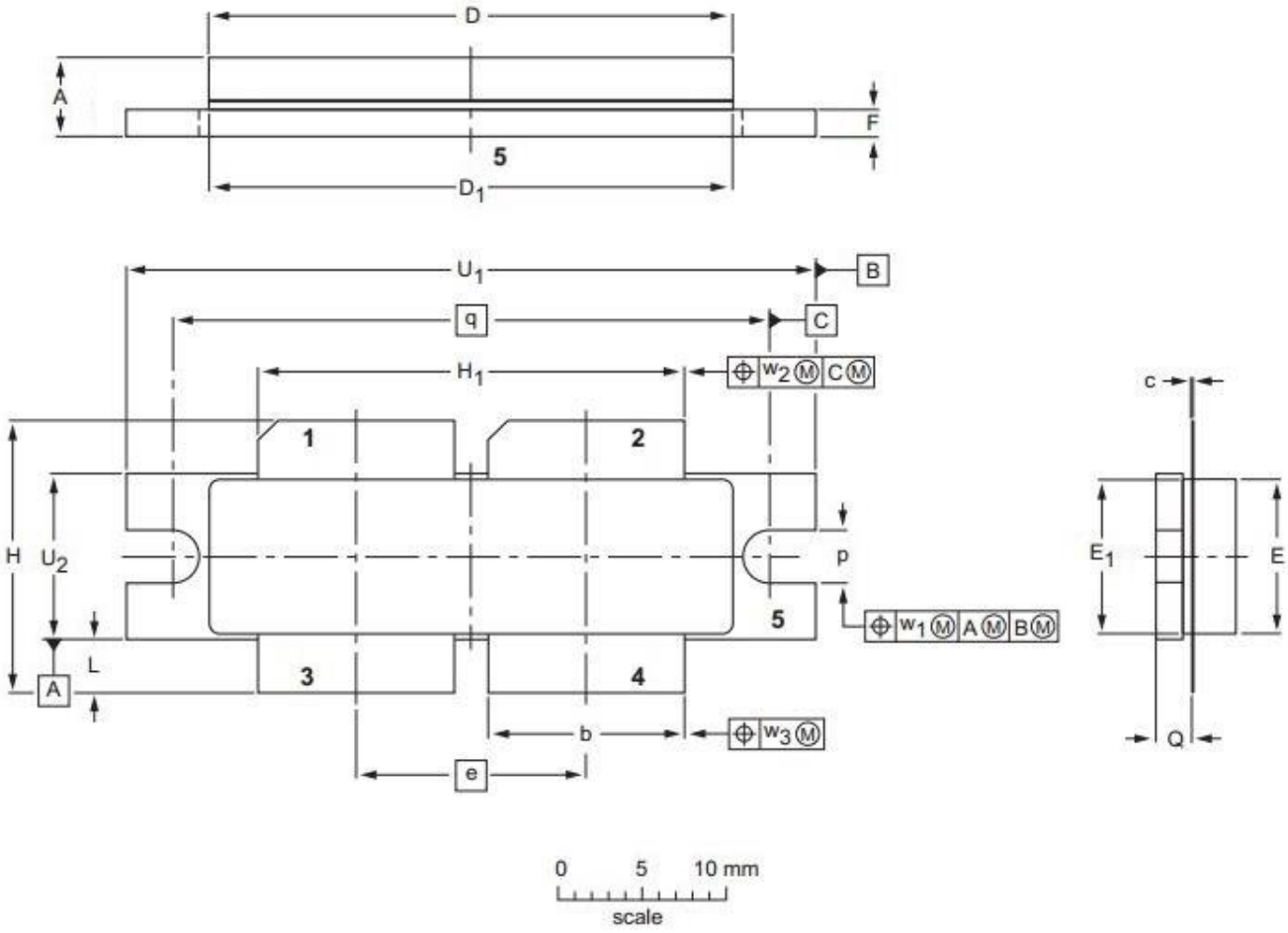
Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	V_{GS}(th)	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 400 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.1	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		108		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		430		pF

Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		100.7		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.59		pF

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/04/20	Rev 1.0	Preliminary Datasheet
2018/9/27	Rev 1.1	Update on power rating, Upper frequency limits, and Rth
2019/12/25	Rev 1.2	Update on upper frequency limits, add FM test data according to RC design

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