



2100-2200MHz, 250W, 28V High Power RF LDMOS FETs

Description

The ITCH22250C2 is a 250-watt, internally matched LDMOS FET, designed for multicarrier WCDMA/PCS/DCS/LTE base station and ISM applications with frequencies from 2100 to 2200MHz. It can be used in Class AB/B and Class C for all typical cellular base station modulation formats.



• Typical Performance (On Innegration fixture with device soldered):

VDD = 28 Volts, IDQ = 800 mA, Pulse CW, Pulse Width=20 us, Duty cycle=10% .

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2110	53.91	246.3	47.9	14.64	54.9	309.0	51.1
2140	53.34	215.5	46.9	14.9	54.41	275.9	50.6
2170	52.92	195.7	45.7	14.88	54.01	252.0	50.4

Typical WCDMA 1 carrier Performance (On Test Fixture with device soldered):

VDD=28Volts, IDQ = 1600 mA,

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Eff (%)
2110	46.01	8.77	54.77	300.1	-30.7	15.4	23.9
2140	46.01	8.41	54.42	277.0	-31.7	15.8	25.2
2170	46.00	8.10	54.09	256.7	-32.6	15.8	26.0

Features

- High Efficiency and Linear Gain Operations
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Integrated ESD Protection
- Pb-free, RoHS-compliant
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCl drift

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	70	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j =200°C, DC test	R _{θJC}	0.27	°C/W



Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =1mA)	V _{DSS}	65	70		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{DSS}			10	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}			1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 600 uA)	V _{GS(th)}		1.8		V
Gate Quiescent Voltage (V _{DD} = 28 V, I _{DQ} = 1600 mA, Measured in Functional Test)	V _{GS(Q)}	2.3	2.8	3.3	V

Functional Tests (On Innogrations demo, 50 ohm system) :V_{DD} = 28 Vdc, I_{DQ} = 800 mA, f = 2110MHz, Pulse CW, Pulse Width=20 us, Duty cycle=10% .

Power Gain @P1dB	G _p		15		dB
1 dB Compression Point	P _{-1dB}		240		W
3dB Compression Point	P _{-3dB}		300		W
Drain Efficiency@P3dB	η _p		50		%
Input Return Loss	IRL		-7		dB

Load Mismatch (On Innogrations Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 800mA, f = 2110 MHz

VSWR 10:1 at 250W pulse CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram

RO4350B, 20mil, Layout file upon request

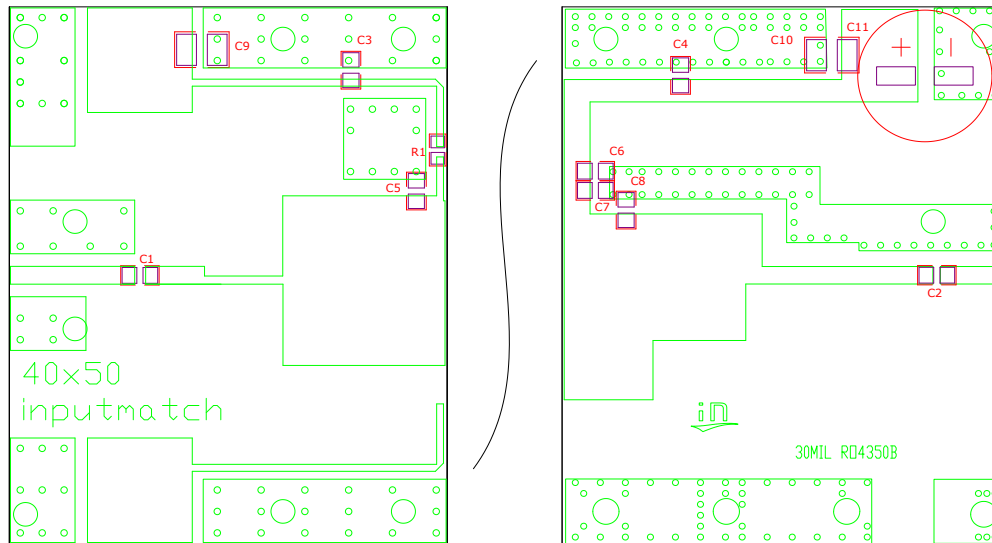


Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1, C2, C3, C4	18pF	0805	4
C5, C7, C8	0.5 pF	0805	3
C6	1.0 pF	0805	1
C9, C10	10uF/100V	1210	2
C11	100uF/63V		1
R1	10ohm	0603	1



TYPICAL CHARACTERISTICS

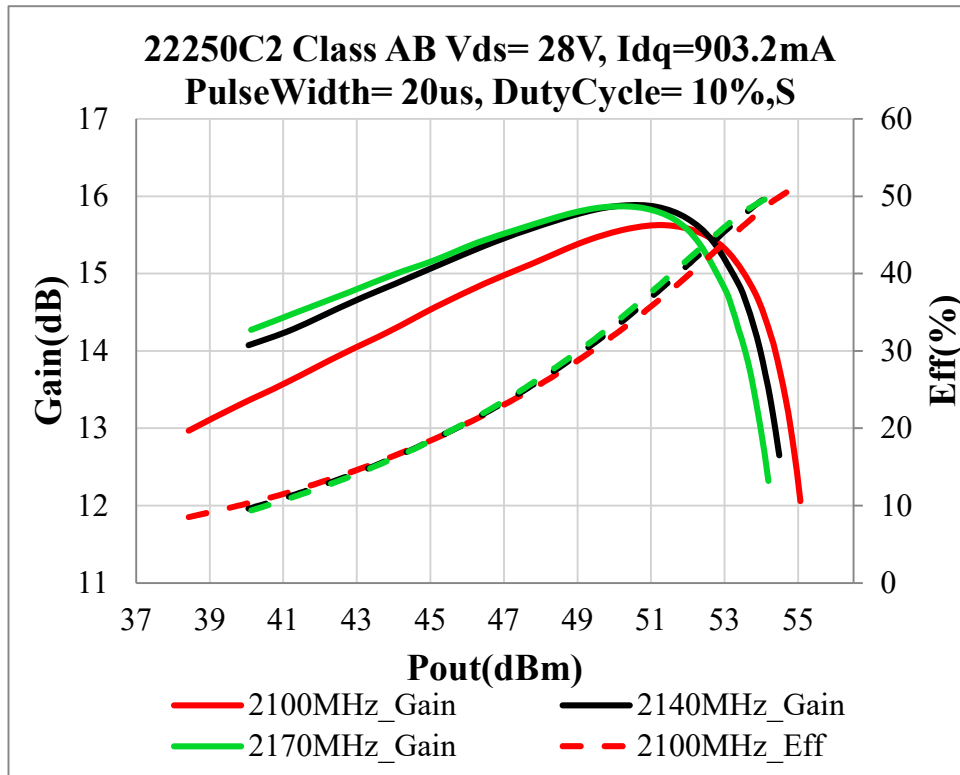


Figure 2. Power gain and drain efficiency as function of Pulse output power (2110-2170MHz)

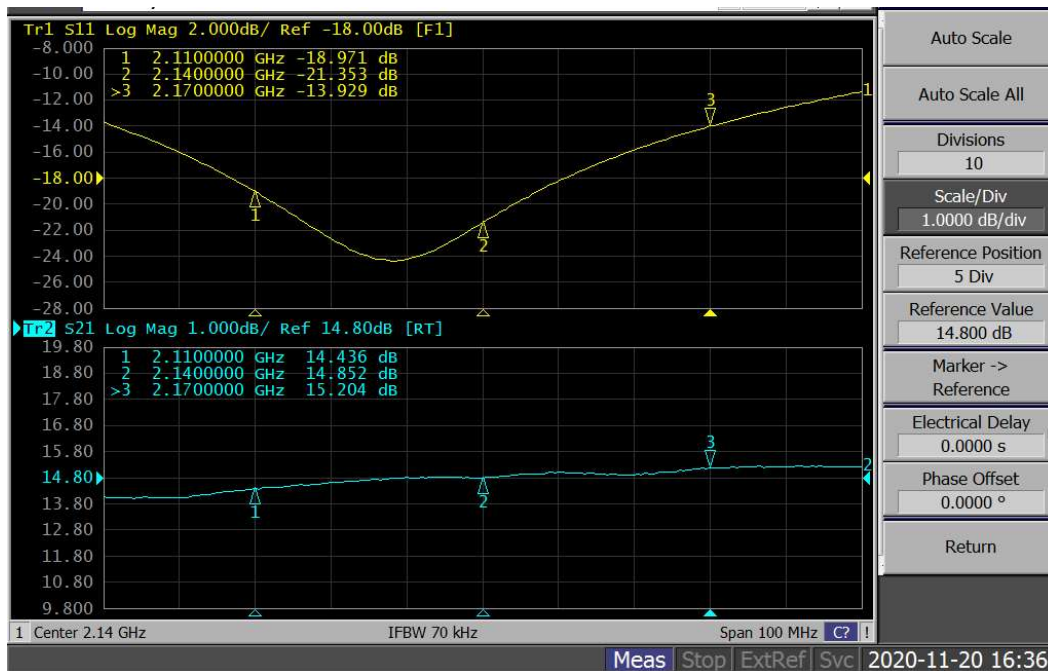
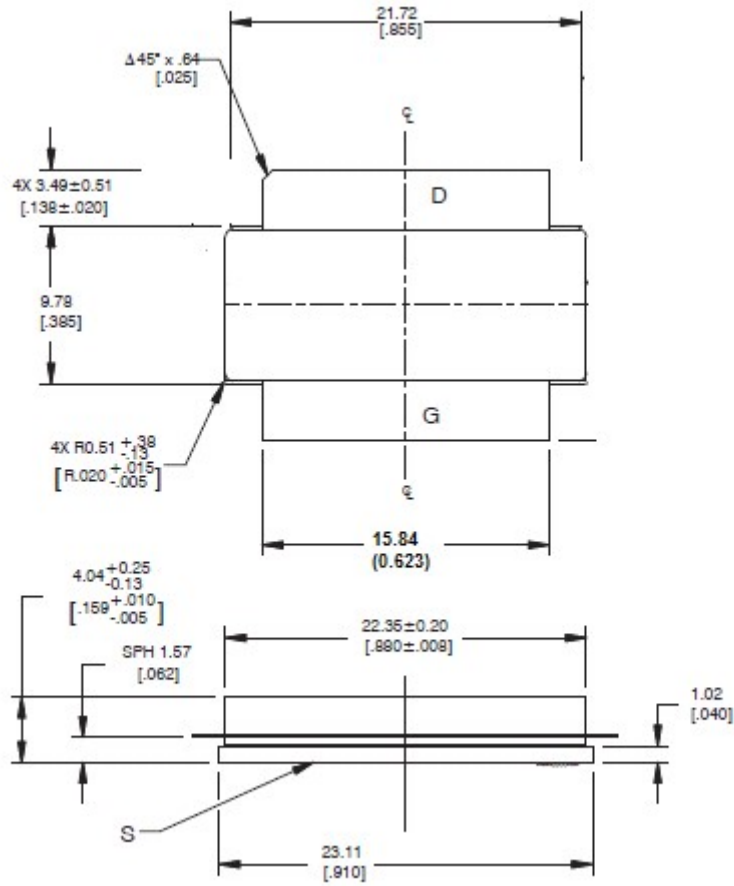


Figure 3. Network analyzer output S11/S21, $I_{dq}=1.6A$



Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2020/11/23	Rev 1.0	Preliminary Datasheet

Application data based on LSM-20-25

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