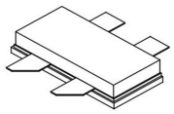
Gallium Nitride 50V, 250W,2.45GHz RF Power Transistor

Description

The STAV25250BY4 is a dual path 250watt, GaN HEMT, ideal for ISM applications at 2.45GHz. Each path is a single stage input matched transistor capable of delivering Psat 140W across the full band. It can support CW, pulse and linear applications.

There is no guarantee of performance when this part is used outside of stated frequencies.

STAV25250BY4



- Typical pulse CW performance across the band with device soldered

V_{DD} = 50 Vdc, Vgs(A+B)=-3.4V, Idq=10mA Pulse width=20us, duty cycle=10%, Tc=25°C, air cooling

Freq(MHz)	P1(dBm)	P3(dBm)	P3(W)	Eff(%)@P3
2400	54.57	55.00	316	72.25
2450	54.26	54.76	299	73.15
2500	53.71	54.46	279	73.77

- Typical CW performance across (2450+/-50MHz) with device soldered

V_{DD} = 50 Vdc, Vgs(A+B)=-3.4V, Idq=10mA, air cooling

Freq(MHz)	Psat(W)	Psat(dBm)	Ids(A)	Gain@Psat (dB)	Eff(%)@Psat
2400	300.6	54.78	8.5	16.00	70
2450	288.4	54.60	8.1	15.80	71
2500	270.4	54.32	7.5	15.60	72

Applications

- Doherty amplifier within 2.3-2.4GHz
- 2.45GHz RF Energy

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

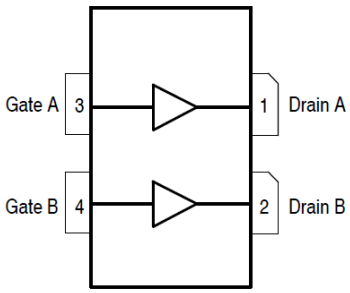


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	36	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=115W	$R_{\theta JC}$	1	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=18mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 18mA	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=10mA, Measured in Functional Test	$V_{GS(Q)}$		--3.4		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.45GHz, Pout=250W pulse CW All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

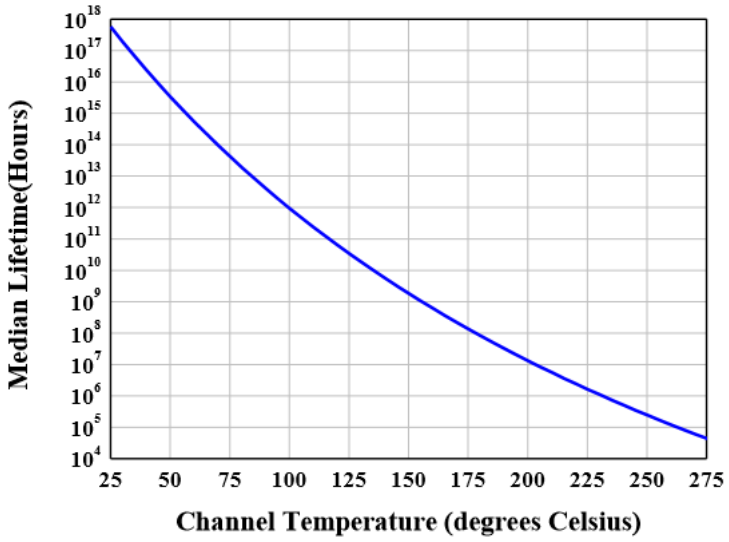
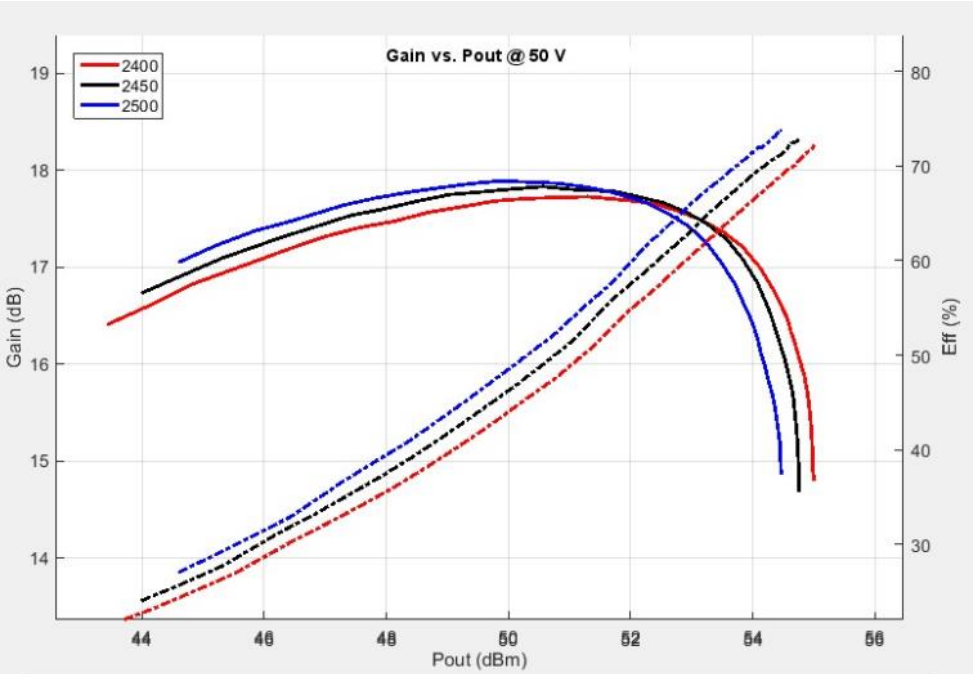


Figure 3: Efficiency and power gain as function of Pout

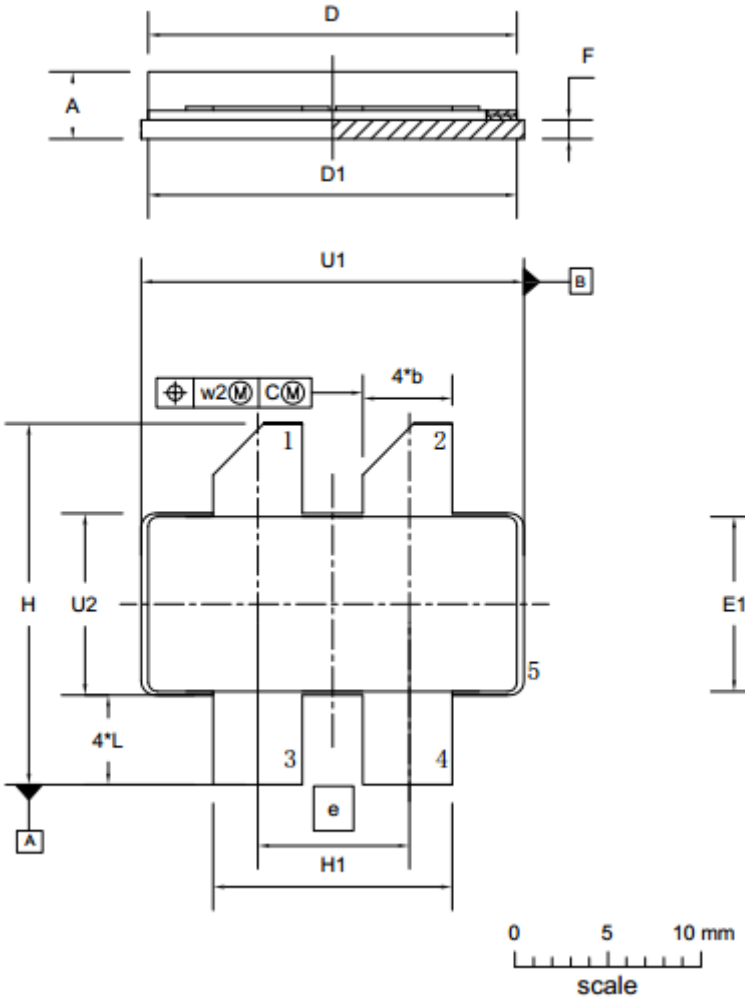
(V_{DD} = 50 Vdc, I_{DQ} = 10mA, Pulse width=20us, duty cycle=10%)



Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2400	54.57	286.29	69.58	16.47	55.00	316.27	72.25
2450	54.26	266.97	70.35	16.56	54.76	299.48	73.15
2500	53.71	234.91	69.93	16.83	54.46	279.53	73.77

Figure 4: S11/S21 output from Network analyser (VDS= 50V, IDQ=210 mA Vgs =-3.1V)

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2020/12/16	**V1.0**	**Preliminary Datasheet Creation**

Application data based on: LWH-20-40

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