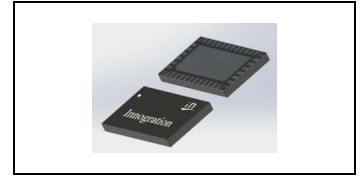




4.6-5.0GHz, 35W, 28V GaN PA Module

Description

The GMAH4650-35 is a 35-watt peak power, integrated 2-stage Power Amplifier Module, designed for massive MIMO applications, with frequencies from 4.6 to 5.0 GHz. The module is 50 Ω input and output and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions. The module incorporates a Doherty final stage delivering high power added efficiency for the entire module at 5.6 W average power.



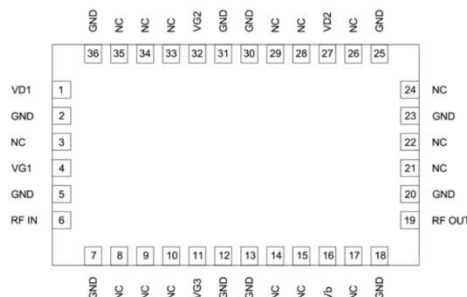
• Typical 1C WCDMA Performance of Doherty Demo (On Innegration fixture with device soldered through grounding vias):

VDS= 28V, Vdriver=-2.38V (30mA) , Vmain=-2.19V(50mA), Vpeak=-4.2V					
Pout(dBm)	Freq (MHz)	Ppeak(dBm)	Gain (dB)	EFF (%)	ACPR (dBc)
37.5	4600	46.20	27.5	39.8	-27.1
	4700	46.30	28.5	41.2	-26.6
	4800	46.19	29.1	41.0	-28.5
	4900	46.18	29.0	41.0	-31.0
	5000	46.24	28.4	39.9	-31.8
VDS= 26V, Vdriver=-2.38V (30mA) , Vmain=-2.19V(50mA), Vpeak=-4.2V					
Pout(dBm)	Freq (MHz)	Ppeak(dBm)	Gain (dB)	EFF (%)	ACPR (dBc)
36.0	4600	45.41	27.2	37.1	-27.8
	4700	45.53	28.1	38.5	-27.6
	4800	45.40	28.5	38.4	-29.3
	4900	45.27	28.3	38.0	-31.1
	5000	45.46	27.5	37.5	-30.9

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- 50 Ω Input / Output
- Integrated Doherty Final Stage
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Pin Configuration and Description





Pin No.	Symbol	Description
1	VD1	Driver Amplifier, Drain Bias
4	VG1	Driver Amplifier, Gate Bias
6	RF IN	RF Input
11	VG3	Carrier Amplifier, Gate Bias
16	Vb	VBW Enhancement Lead
19	RF OUT	RF Output
27	VD2	Peaking Amplifier, Drain Bias
32	VG2	Peaking Amplifier, Gate Bias
3,8-10,14-15,17,21,22,24,26,28,29,33-35	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36	GND	Internal Grounding, recommend connecting to Epad ground
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	150	Vdc
Gate--Source Voltage	V_{GS}	-10 to +2	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance@Average Power, Junction to Case $T_{case}=+85^{\circ}C$, $T_{ch}=126.5^{\circ}C$, CW Test, $P_{diss}=9W$, $P_{out}=5W$,	$R_{\theta JC}$	4.6	°C/W

Notes:

- (1) The thermal resistance is acquired by our company's FEA model, which was calibrated by IR measurement, the value shall be applied to reliability.
- (2) The reference T_{case} temperature $85^{\circ}C$ is apply on the backside of package.
- (3) If the device soldering onto the 20mil Rogers PCB with $50 \times \Phi 0.4mm$ via hole beneath the package backside and the reference temperature T_{case} ($85^{\circ}C$) apply on the groundside of the PCB, the total thermal resistance $R_{\theta JC}=TBD^{\circ}C/W$.
- (4) The power dissipation in the table is overall dissipation which include Carrier PA, Peaking PA and driver PA.

Table 3. ESD Protection Characteristics

Test Methodology	Class Voltage
Human Body Model(HBM) (JEDEC Standard JESD-A114)	$\pm 225V$
Charged Device Model (CDM) (JEDEC Standard JESD22-C101F)	$\pm 1000V$

Table 4. Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		4.6		5.0	GHz
Driver Quiescent Current (I_{DQ1})			30		mA
Carrier Quiescent Current (I_{DQ3})			50		mA
Peak PA Gate Quiescent Voltage (V_{G2})			-4.2		V



Power Gain @ P1dB	Freq=5.0GHz	28.3	dB
P1dB	Freq=5.0GHz	44.8	dBm
P3dB	Freq=5.0GHz	45.5	dBm
Drain Efficiency@ P3dB	Freq=5.0GHz	55.5	%

Unless otherwise noted: TA = 25°C, V_{D1,2} =28 V, Pulse Width=20 us, Duty cycle=10%

Load Mismatch of per Section (On Test Fixture, 50 ohm system): V_{D1,2} =28 V, I_{DQ1} =30 mA, I_{DQ3} =50 mA, V_{G2} =-4.1V, f = 5.0 GHz

VSWR 10:1 at P3dB pulse CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram

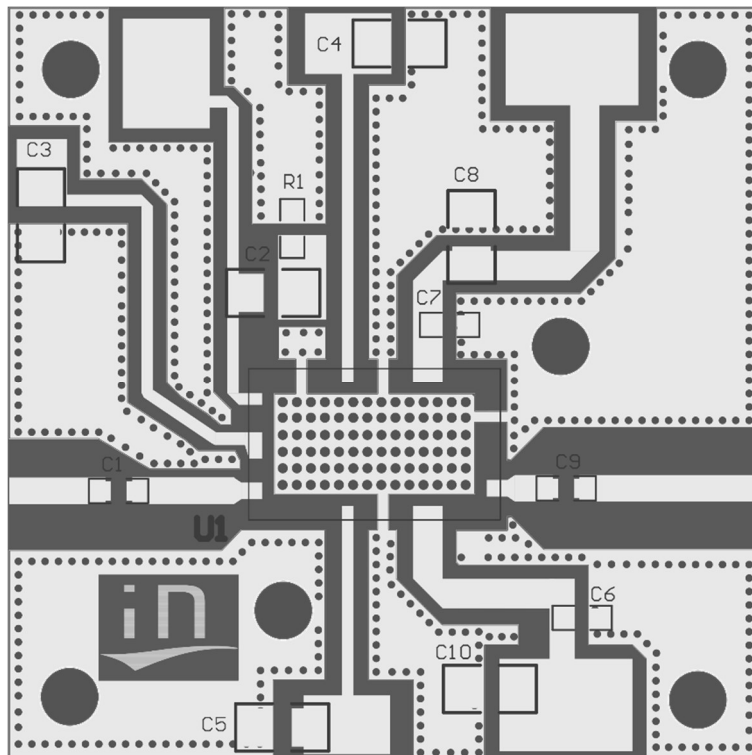


Figure 1. Test Circuit Component Layout

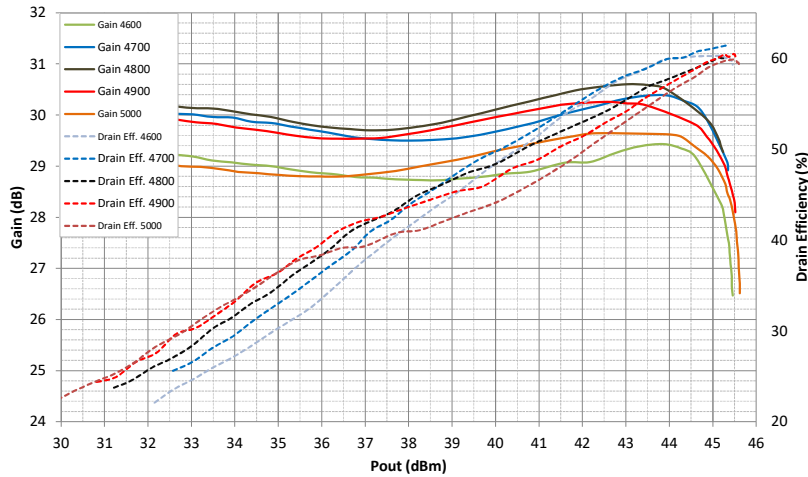
Table 5. Test Circuit Component Designations and Values

Component	Value	Description
U1	GMAH4650_35	35W PA Module
R1	10 Ω	0603
C1、C6、C7、C9	3.9pF	ATC600S
C2、C3、C4、C5、C8、C10	10uF	TDK1206



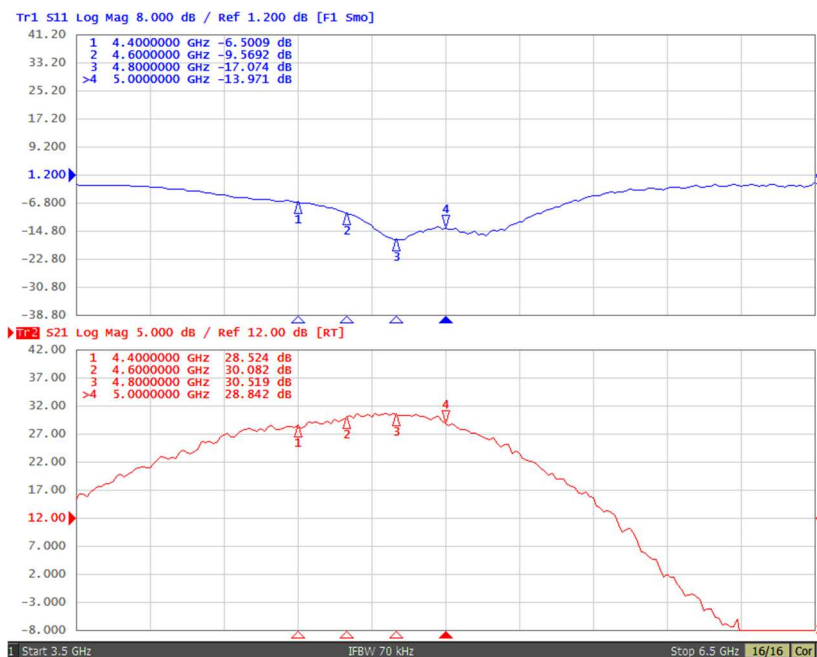
TYPICAL CHARACTERISTICS

Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power



VDS= 28V, Vdriver=-2.38V (30mA) , Vmain=-2.19V(50mA), Vpeak=-4.2V					
Freq (MHz)	P1(dBm)	P1 Gain (dB)	P3dB(dBm)	P3dB(W)	EFF (%)
4600	45.19	28.3	45.46	35.1	59.3
4700	45.26	29.2	45.56	36.0	60.6
4800	45.13	29.5	45.53	35.8	59.5
4900	45.27	29.0	45.62	36.5	60.0
5000	45.29	28.7	45.62	36.5	59.1

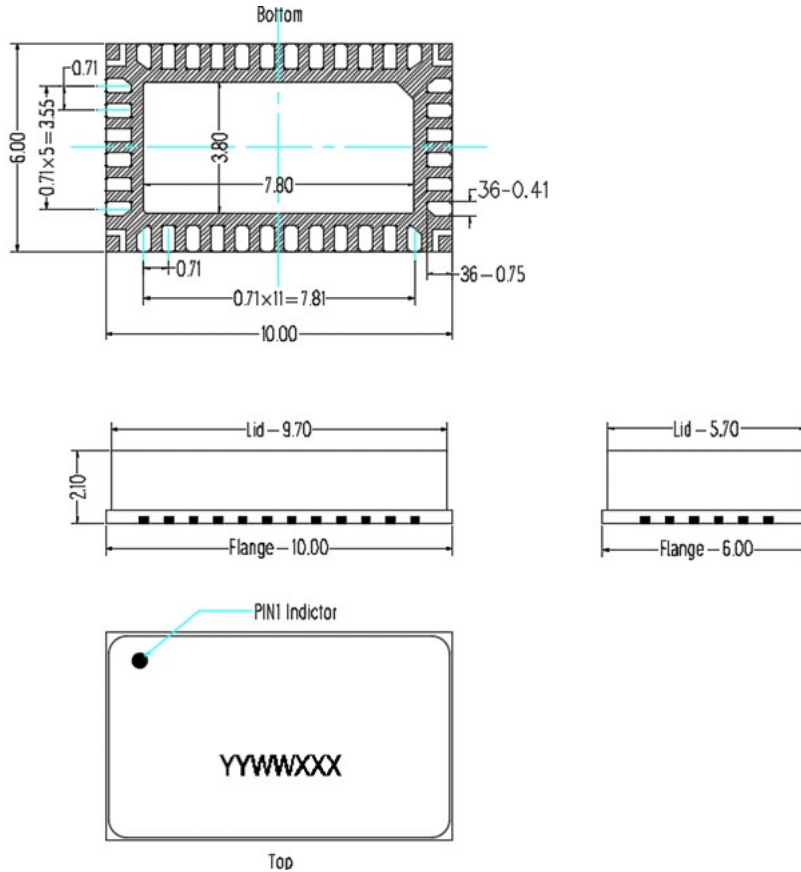
Figure 2. S11/S21 output from Network analyzer





Package Dimensions

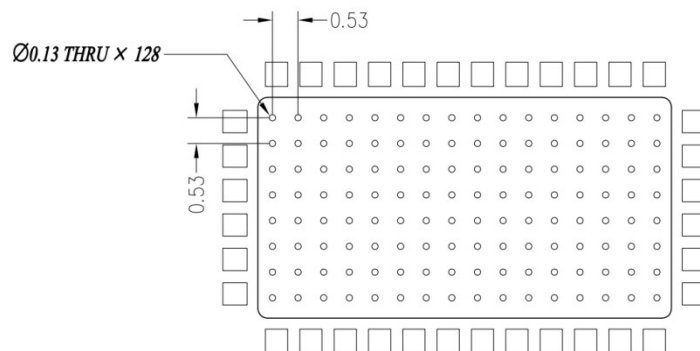
10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2020/09/14	Rev 1.0	Objective Datasheet, based on estimated performance from available GMAH4850-35
2020/9/18	Rev 1.0	Preliminary datasheet creation

Application data based on HJ-20-19

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