



Gallium Nitride 50V, 200W, 3.3-3.6GHz RF Power Transistor

Description

The STAV36200AY2 is a single ended 200watt, GaN HEMT, ideal for applications from 3.3 to 3.6GHz.

It is an input matched transistor capable of delivering Psat 225W.

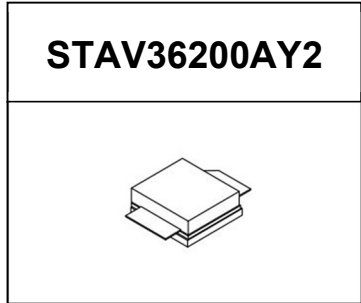
It can support CW, pulse or any modulated signal.

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical pulse CW performance across 3.3-3.6GHz

V_{DD} = 48 Vdc, I_{DQ} = 210mA, Pulse width=20us, duty cycle=20%, T_c=25°C

(On innogrations application board with device soldered)



Frequency	P3dB(W)	Eff(%)@P3dB
3300	230	56
3450	220	57
3600	202	57

- WCDMA 3GPP TM1 64 DPCH 9.9 dB PAR @ 0.01% CCDF. V_{DS} = 48 V, I_{DQ} = 210 mA, P_{OUT} = 44W across 3.3-3.6G

(On innogrations Class AB application board with device soldered)

Freq(MHz)	Pout(dBm)	CCDF(dB)	Ppeak(dBm)	Ppeak(W)	ACPR(dBc)	Gain(dB)	Efficiency(%)
3300	46.43	7.17	53.60	228.86	-35.90	13.37	29.73
3450	46.47	6.98	53.44	221.05	-34.91	13.03	30.90
3600	46.45	6.79	53.24	210.89	-33.68	13.43	32.68

Applications

- Sub-4GHz pulse or CW amplifier
- 5G base station amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set V_{GS} to the pinch-off (V_P) voltage, typically -5 V
2. Turn on V_{DS} to nominal supply voltage
3. Increase V_{GS} until I_{DS} current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce V_{GS} down to V_P, typically -5 V
3. Reduce V_{DS} down to 0 V
4. Turn off V_{GS}

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

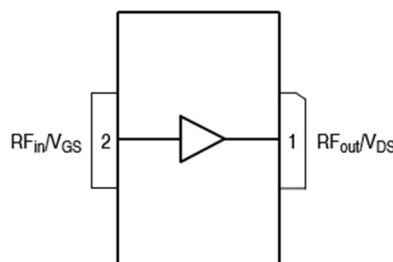




Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	25	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 85^\circ\text{C}$, at $P_d = 80\text{W}$	$R_{\theta JC}$	1.8	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 25\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 25\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 210\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	3.45GHz, $P_{out} = 200\text{W}$ pulse CW for each path All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

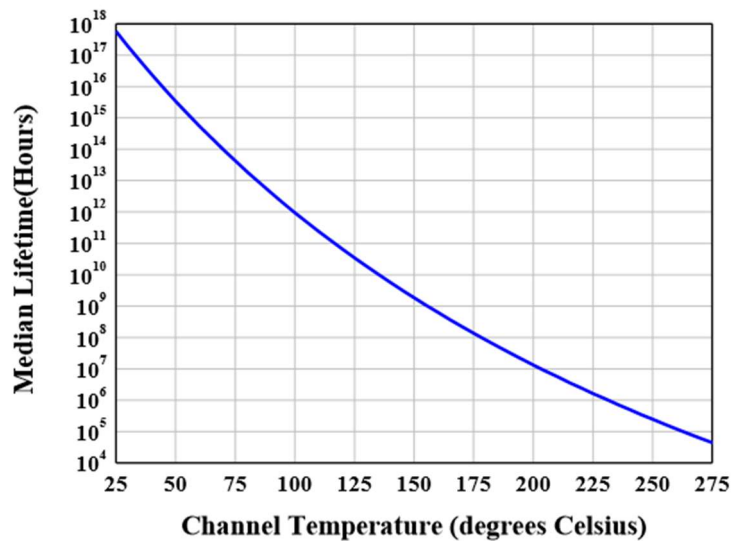




Figure 3: Efficiency and power gain as function of Pout

(VDD = 48Vdc, IDQ = 210 mA, Pulse width=20us, duty cycle=20%)

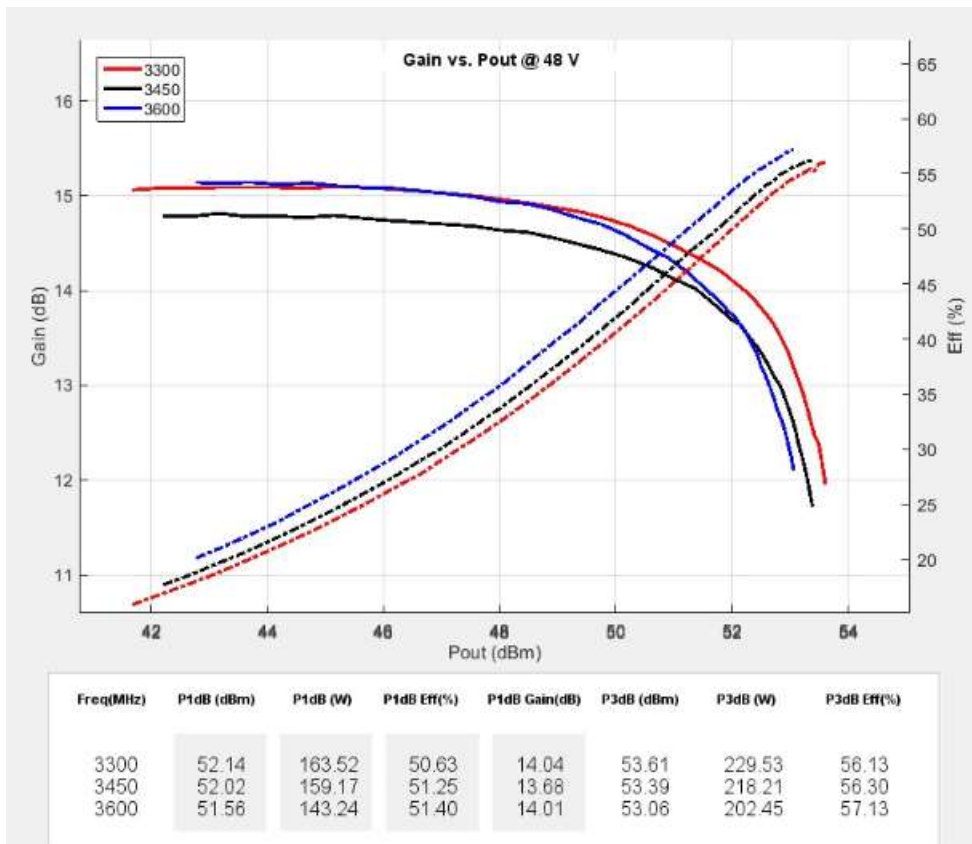


Figure 4: S11 / S21 output from network analyzer

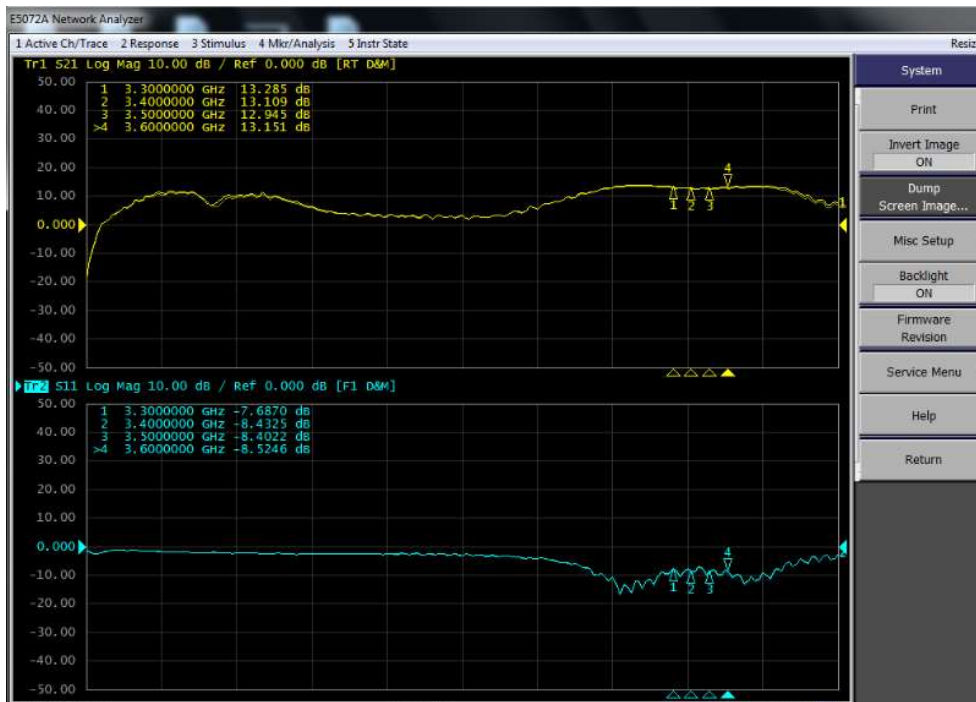


Figure 5: Picture of application board of 3.3-3.6GHz

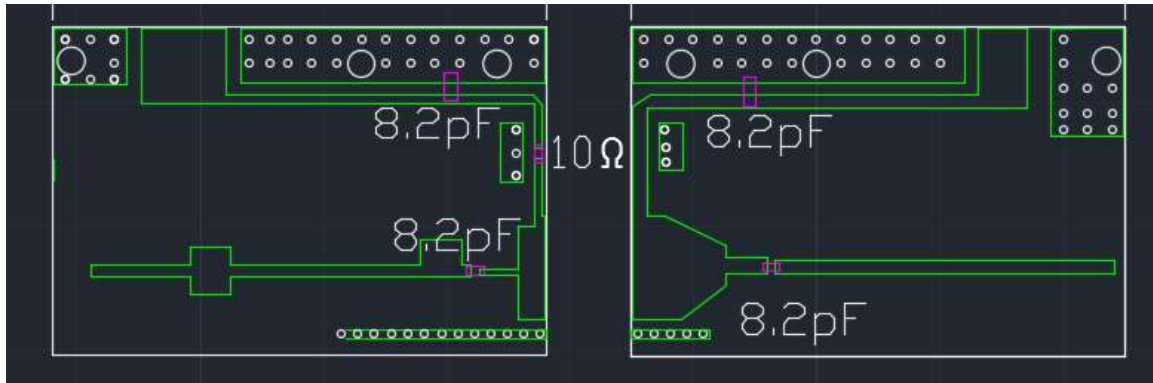
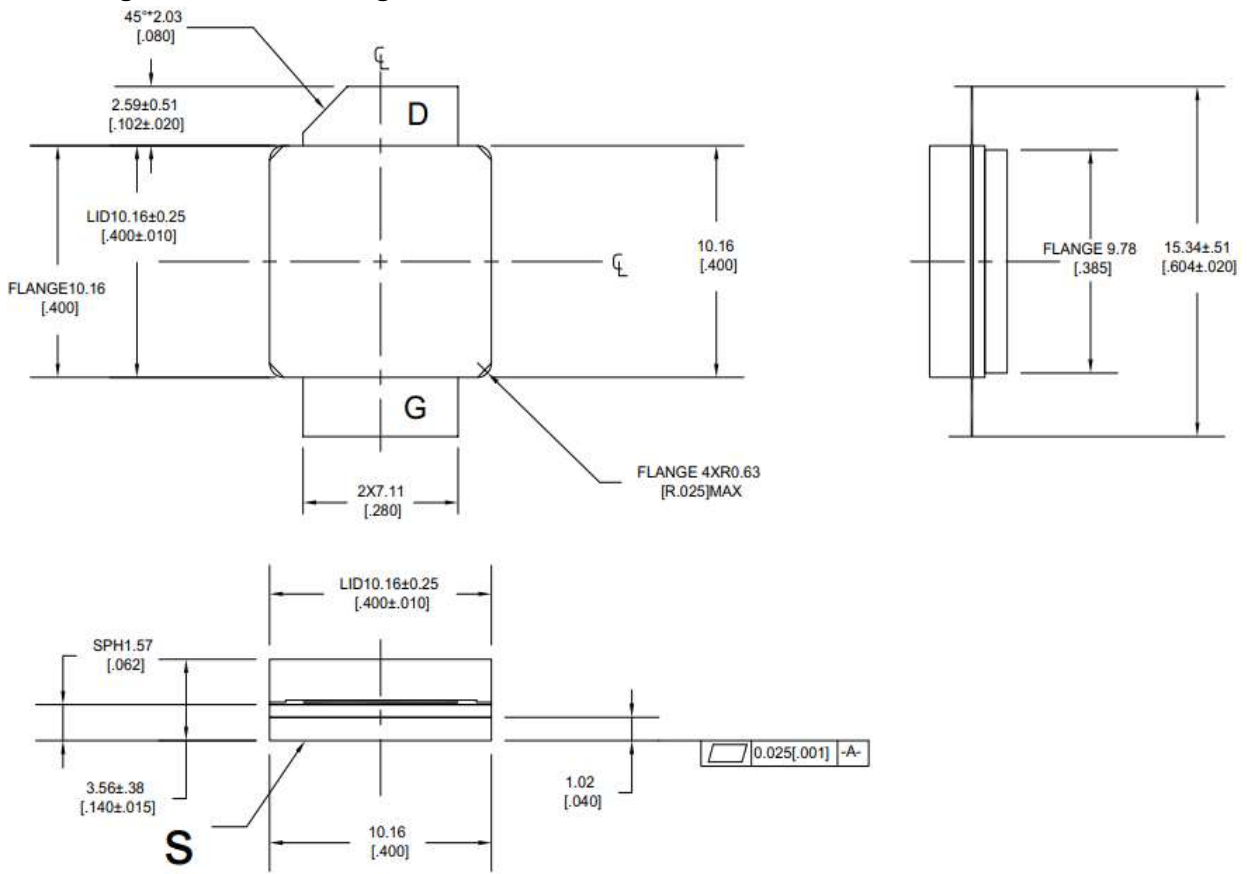


Table 4. Bill of materials of application board (PCB layout upon request)

BOM		
C1,C2,C3,C4	8.2pF	ATC600F
C5,C6	10uF/63V	
C7	470uF/63V	
R1	10 ohm	



Earless Flanged Ceramic Package; 2 leads



Unit: mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2020/3/27	V1.0	Preliminary Datasheet Creation

Application data based on: LWH-20-05

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