

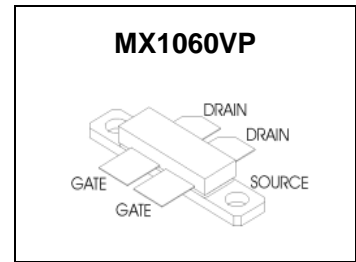
MX1060VP LDMOS TRANSISTOR

Document Number: MX1060VP
Preliminary Datasheet V1.0

600W, 50V High Power RF LDMOS FETs

Description

The MX1060VP is a 600-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1.0 GHz.



- Typical performance(on Innogration test board with device soldered)

Signal: CW, $V_{ds}=36V$, $I_{dq}=200mA$

Freq (MHz)	Pout (W)	Gain (dB)	Effi (%)
30	300	16	79%
100	300	19.5	66%
200	300	19.1	59%
300	300	16.8	51%
400	300	17.5	51%
512	300	16.8	56%

- Typical performance(on Innogration test board with device soldered)

Signal: CW, $V_{ds}=28V$, $I_{dq}=200mA$

Freq(MHz)	Psat(W)	Gp(dB)	Eff(%)
30	200	13.2	81%
60	211	16.55	77%
100	213	17.0	69%
150	218	16.4	63%
200	213	17.0	61%
250	200	15.1	57%
300	200	15.4	51%
350	213	15.6	50%
400	223	15.7	53%
450	218	15.8	56%
512	204	14.6	55%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

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- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	28~50	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 1.0\text{Ma}$	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	---	---	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	---	---	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	---	2.65	---	V
Gate Quiescent Voltage ($V_{DD} = 50\text{V}$, $I_D = 200\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	---	3.25	---	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system):

Load Open, All phase angles, at 500W Pulsed CW Output Power	Condition: $V_{DD} = 50\text{V}$, $I_{DQ} = 200\text{mA}$, $f = 500\text{MHz}$, pulse width:100us, duty cycle:10%	No Device Degradation
Load Open, All phase angles, at 300W CW Output Power,	Condition: $V_{DD} = 36\text{V}$, $I_{DQ} = 200\text{mA}$, $f = 30\sim 500\text{MHz}$	No Device Degradation

TYPICAL CHARACTERISTICS

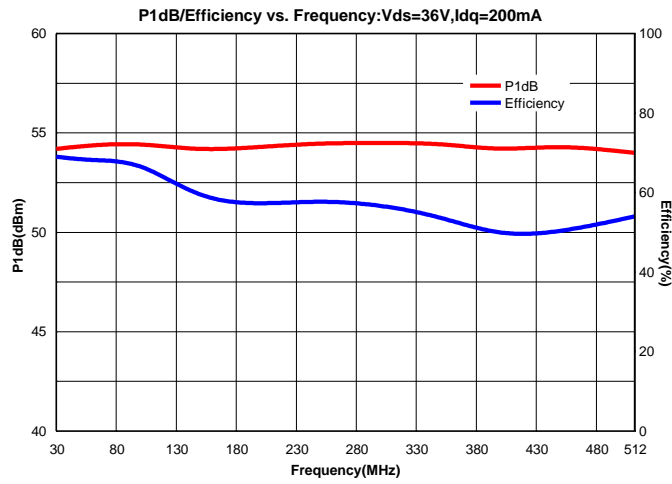


Figure 2: CW P1dB as function of Frequency (36V)

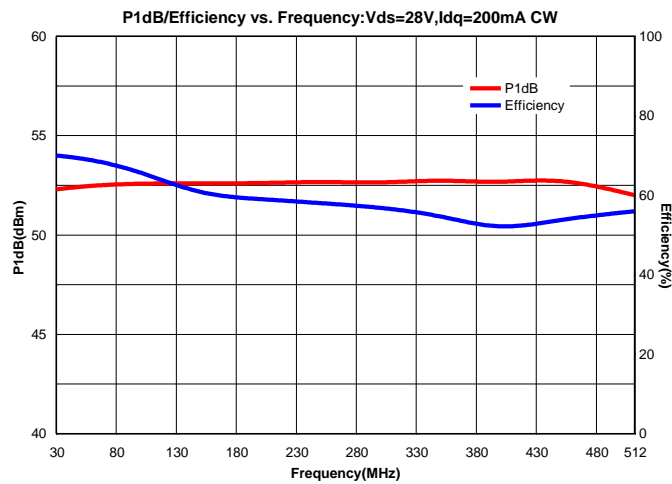


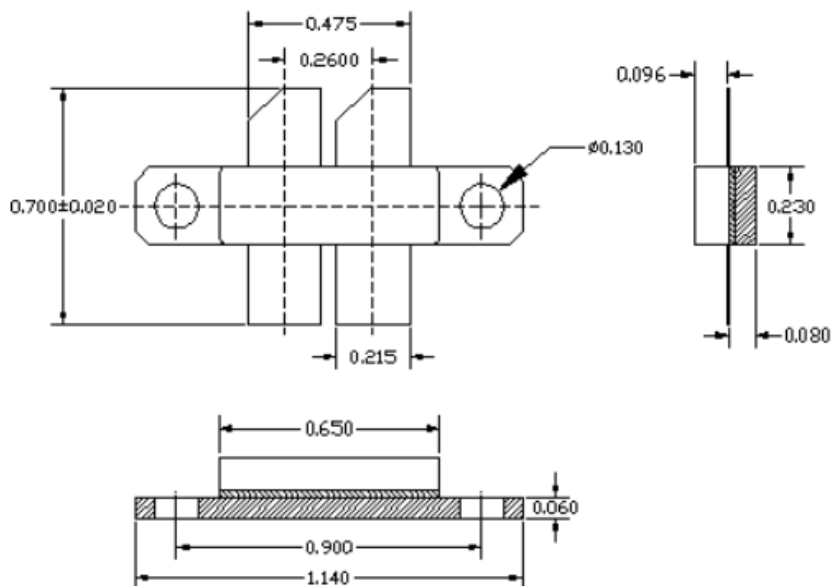
Figure 2: CW P1dB as function of Frequency (28V)

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Tolerance .XX +/-0.01 .XXX +/- .005 inches

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/08/10	Rev 1.0	Preliminary Datasheet Creation

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