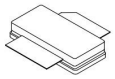
700-1700MHz, 180W, 28V High Power RF LDMOS FETs

Description

The ITCH16180B2 is a 180-watt, internally matched LDMOS FET, designed for multicarrier WCDMA/PCS/DCS/LTE base station and ISM applications with frequencies from 700 to 1700 MHz. It Can be used in Class AB/B and Class C for all typical cellular base station modulation formats.

ITCH16180B2



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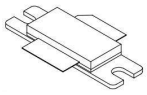

•Typical Performance (On Innogration fixture with device soldered):

VDD = 28 Volts, I_{DQ} = 800 mA, Pulse CW, Pulse Width=12 us, Duty cycle=10% .

Frequency	Gp (dB)	P_{-1dB} (dBm)	η_D@P_{-1} (%)	P_{-3dB} (dBm)	η_D@P_{-3} (%)
1390 MHz	18.8	52.8	55	53.7	57
1450 MHz	19.2	52	54	53.2	57.3
1529 MHz	18.4	51	54	52.2	57.6

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1350 MHz	19.6	52.4	53.5	53.5	57.8
1375 MHz	19.7	52.1	54	53.3	58.2
1400 MHz	19.4	51.7	53.5	53	58

•Typical Performance (On Innogration fixture with device soldered):

VDD = 28 Volts, I_{DQ} = 800 mA, Pulse CW, Pulse Width=12 us, Duty cycle=10% .

Frequency	Gp (dB)	P_{-1dB} (dBm)	η_D@P_{-1} (%)	P_{-3dB} (dBm)	η_D@P_{-3} (%)
1440 MHz	19.8	52.2	55.8	53.2	59
1450 MHz	19.9	51.9	55	53	59
1470 MHz	19.8	51.5	54.9	52.7	59

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C

Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.38	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	65			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_{DQ} = 800 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.7	3.2	V

Functional Tests (In Innogration 1.44-.147GHz-demo, 50 ohm system) :V_{DD} = 28 Vdc, I_{DQ} = 800 mA, f = 1470 MHz, Pulse CW, Pulse Width=12 us, Duty cycle=10% .

Power Gain	G_p		19.8		dB
Drain Efficiency@P3dB	η_D		59		%
1 dB Compression Point	P_{-1dB}		51.5		dBm
3dB Compression Point	P_{-3dB}		52.7		dBm
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 800 mA, f = 1500 MHz

VSWR 10:1 at 180W pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

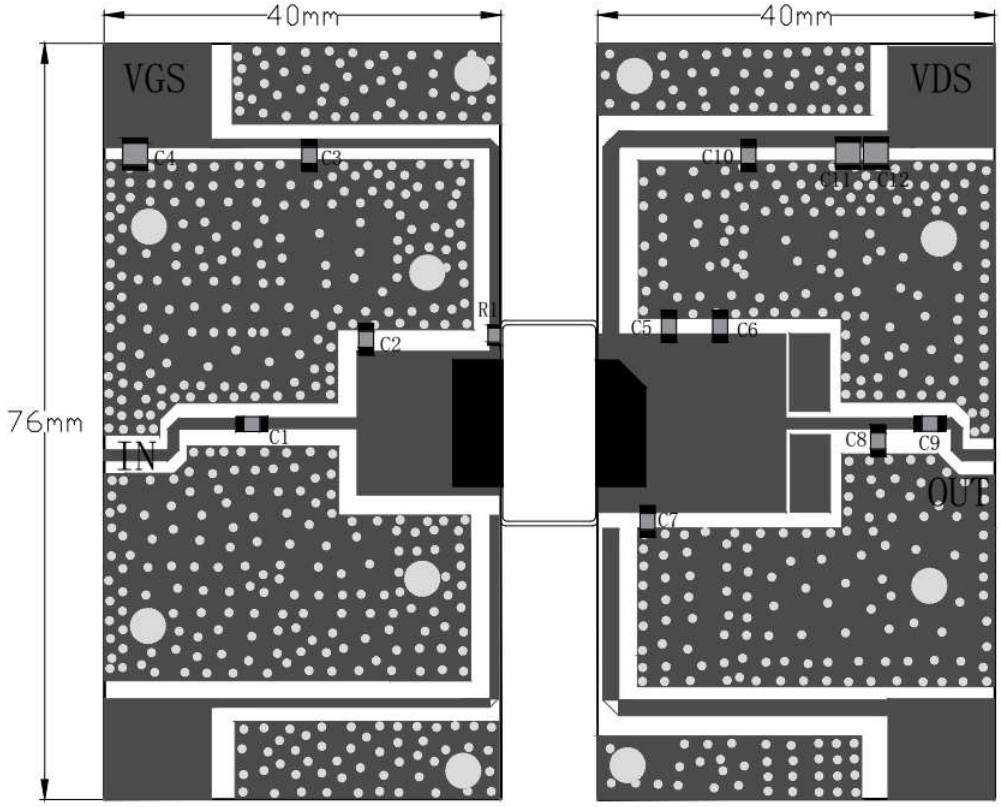


Figure 1. Test Circuit Component Layout (1440MHz~1470MHz)

Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer	P/N
C1	Ceramic Capacitor,30pF	ATC	600F 300
C2	Ceramic Capacitor,2.2pF	ATC	600F 2R2
C3,C10	Ceramic Capacitor,27pF	ATC	600F 270
C5	Ceramic Capacitor,4.7pF	ATC	600F 4R7
C6	Ceramic Capacitor,3.9pF	ATC	600F 3R9
C7	Ceramic Capacitor,5.6pF	ATC	600F 5R6
C8	Ceramic Capacitor,3.0pF	ATC	600F 3R0
C9	Ceramic Capacitor,33pF	ATC	600F 330
C4,C11,C12	Capacitor,10uF	Murata	GRM32DF51H106
R1	Chip Resistor,10 Ω	Digi-Key	P10ECT-ND
PCB	0.76mm [0.030''] thick, εr=3.48, Rogers RO4350, 1 oz. copper		

TYPICAL CHARACTERISTICS

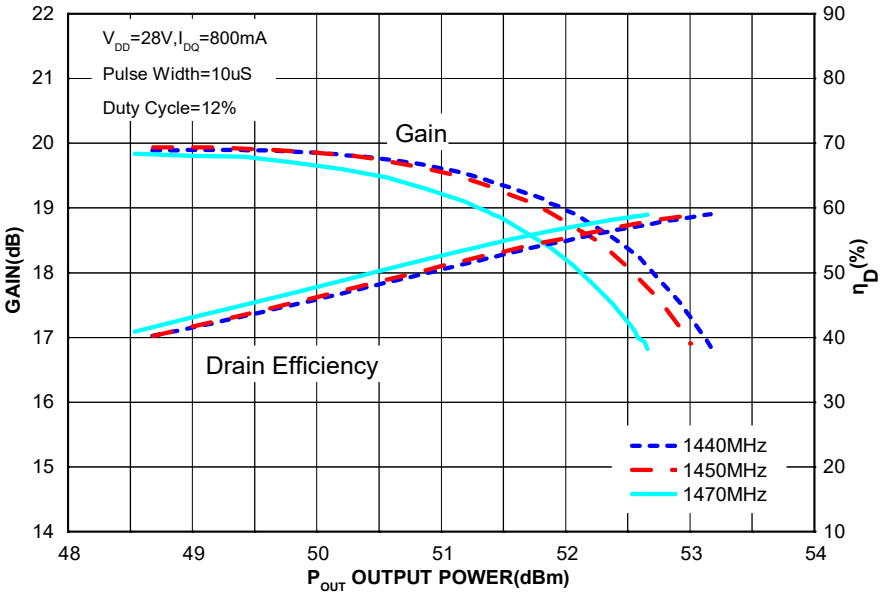
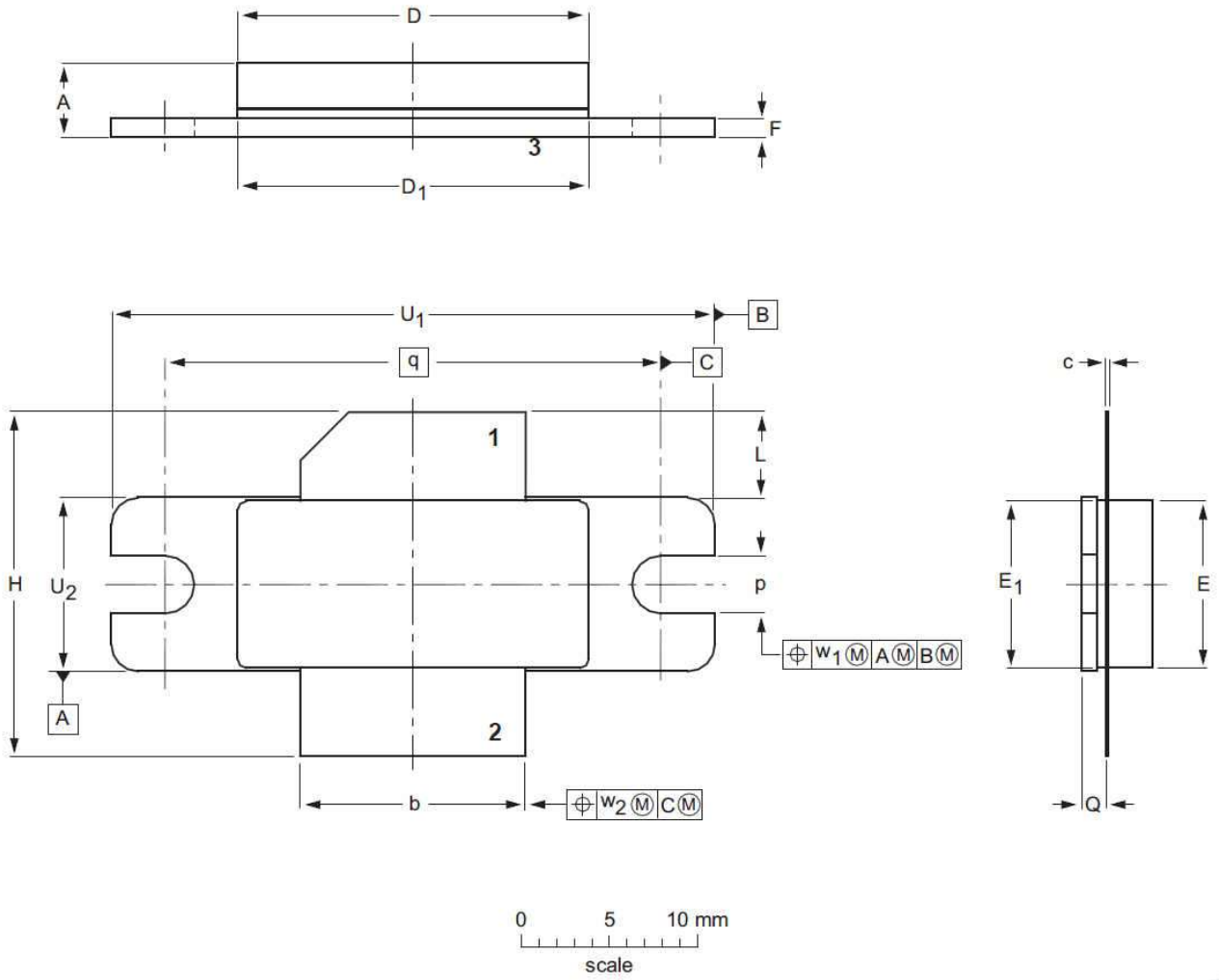


Figure 1. Power gain and drain efficiency as function of Pulse output power（1440-1470MHz）

Package Outline

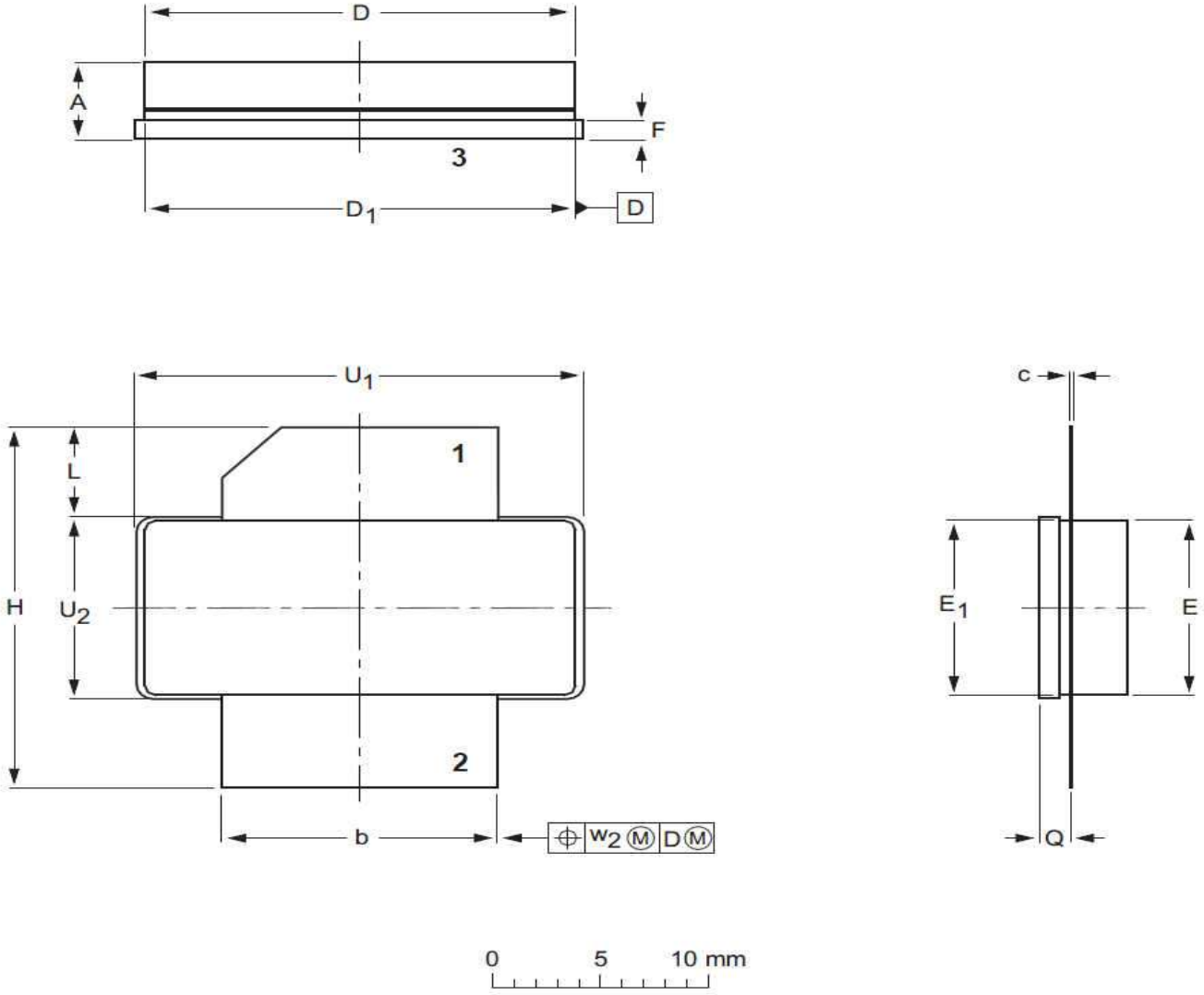
Flanged ceramic package; 2 mounting holes; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2017/01/23	Rev 1.0	Preliminary Datasheet
2017/03/17	Rev 2.0	Preliminary Datasheet
2020/6/21	Rev 2.1	Modify the lower frequency limits

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