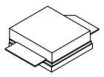
700-1600MHz, 80W, 28V High Power RF LDMOS FETs

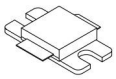
Description

The ITCH16080A2 is a 80-watt, input-matched LDMOS FETs, designed for Beidou Global Positioning System and communication/ISM applications with frequencies from 700 MHz to 1600 MHz. It can be used in Class AB/B and Class C for all typical modulation formats.

ITCH16080A2



ITCH16080A2E



•Typical Performance (On Test Fixture with device soldered):

VDD = 28 Volts, I_{DQ} = 700 mA, Pulse CW, Pulse Width=12 us, Duty cycle=10% .

Frequency	Gp (dB)	P_{1dB} (dBm)	η_D@P_1 (%)	P_{3dB} (dBm)	η_D@P_3 (%)
1447 MHz	19.9	49.1	54.8	50.1	57.9
1457 MHz	20.0	48.8	54.5	49.8	57.6
1467 MHz	20.0	48.3	53.5	49.4	56.7

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	-55~+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 87°C, T_J=175°C, DC test	$R_{\theta JC}$	1.0	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current	I_{DSS}			1	μA

(V_{DS} = 28 V, V_{GS} = 0 V)					
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 450 μA)	$V_{GS(th)}$		2.0		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 700 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.8		V

Functional Tests (In Innogration Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 400 mA, f =1615 MHz, CW Signal Measurements.

Power Gain @ P_{1dB}	Gp		19		dB
1 dB Compression Point	P_{-1dB}		80		W
Drain Efficiency@P_{1dB}	η_D		58		%
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 700 mA, f = 1500 MHz

VSWR 10:1 at 80W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

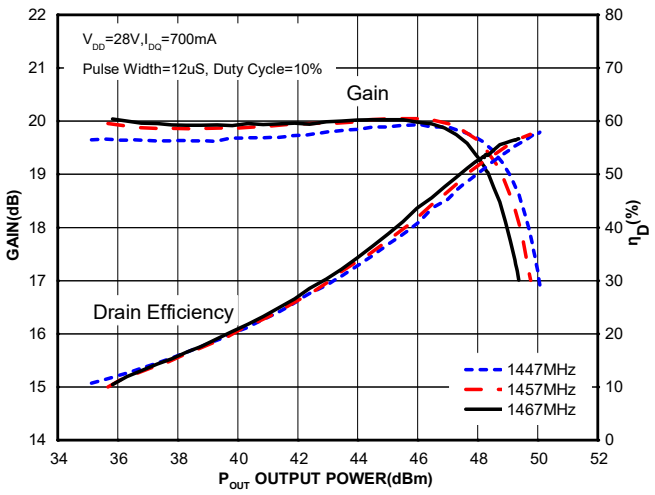
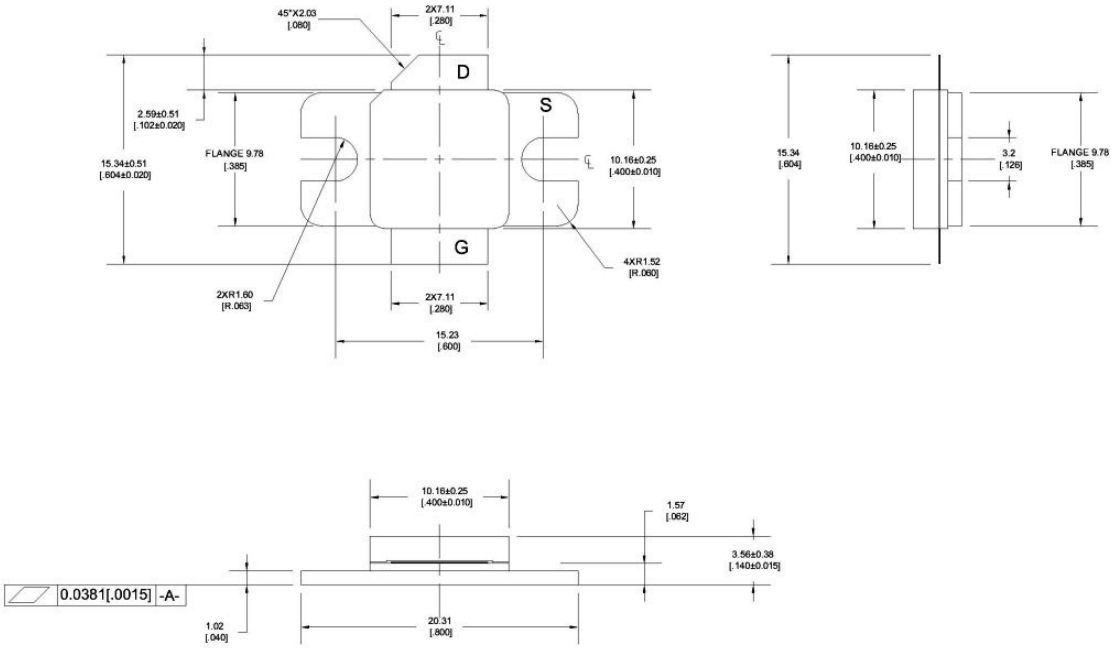


Figure 1. Power gain and drain efficiency as function of average load power(1444-1467MHz)

Package Outline

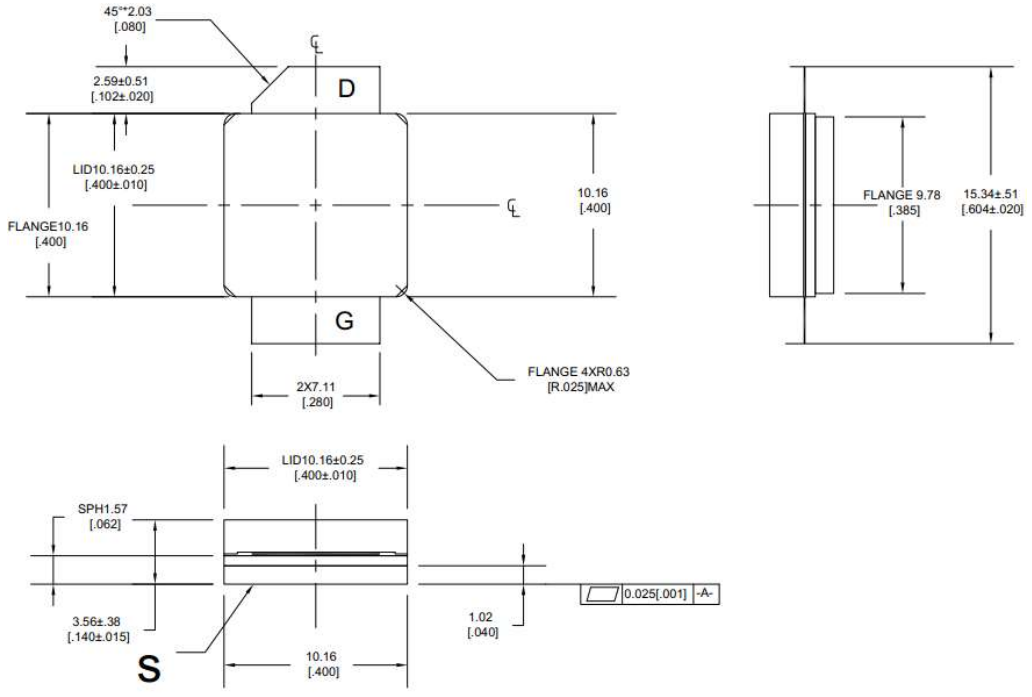
Eared Flanged ceramic package; 2 leads (A2E)



Unit：mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Earless Flanged ceramic package; 2 leads (A2)



Unit：mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/05/24	Rev 1.0	Preliminary Datasheet
2018/09/27	Rev 1.1	Preliminary Datasheet
2020/03/16	Rev 1.2	Preliminary Datasheet
2020/6/21	Rev 1.3	Modify the lower frequency limits

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