Gallium Nitride 28V 12W, RF Power Transistor

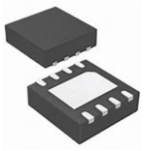
Description

The GTAH35012PD is a 12W GaN HEMT, designed for multiple applications, up to 6000MHz. The transistor is available in a cost effective 4mm*4mm, surface mount, DFN package with 100% DC production test to ensure the quality and consistency.

It can be used in CW, Pulse and multiple modulation mode.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

GTAH35012PD



DFN 4*4mm

- Typical Performance of class AB circuit (On different Innogration fixtures):

V_{DD} =28 V, I_{DQ} =20 mA, Pulse CW, Pulse Width=20 us, Duty cycle=10%.

Freq (MHz)	Pulse CW Signal			
	P_{1dB} (dBm)	Gain@ P_{1dB} (dB)	P_{3dB} (dBm)	η_D@P_3 (%)
915	41.0	20.3	42.1	74
1800-2200	41	17.7	42	70
2300-2700	42	17	42.5	69
3400-3800	41	15	41.7	60
5300-5900	41.3	10	42.4	57

- Typical Performance of class AB circuit (On different Innogration fixtures):

V_{DD} =28 V, I_{DQ} =20 mA, WCDMA 1 carrier CCDF=10dB

Freq (MHz)	Pout=30dBm			
	CCDF (dB)	ACPR (dB)	Gain (dB)	η_D (%)
1800-2200	10	-33	18	22
2300-2700	10	-38	17	20
3400-3800	9.6	-37	15	20
5300-5900	9.7	-37	10.5	15

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

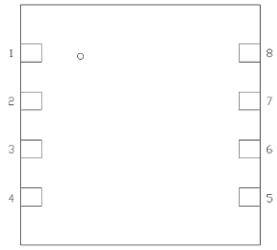
Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (28V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
2, 3	RF IN /VGS	RF Input, Gate Bias
6, 7	RF OUT /VDS	RF Output, Drain Bias
1, 4, 5, 8	NC	No connection
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	125	Vdc
Gate--Source Voltage	V_{GS}	-10,+2	Vdc
Operating Voltage	V_{DD}	40	Vdc
Maximum Forward Gate Current @ T_C = 25°C	Igmax	3	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature(See note 1)	T_J	+200	°C
Total Device Power Dissipation (Derated above 25°C, see note 2)	Pdiss	21	W

Note: 1. Continuous operation at maximum junction temperature will affect MTTF
2.Bias Conditions should also satisfy the following expression: Pdiss < (Tj – Tc) / RJC and Tc = Tcase

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, RF CW operation	$R_{\theta JC}$	5.5	℃/W

Table 3. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=3mA	V_{DSS}		125		V
Gate Threshold Voltage	V_{DS} = 28V, I_D =3 mA	V_{GS}(th)		-2.7		V
Gate Quiescent Voltage	V_{DS} =28V, I_{DS}=20mA, Measured in Functional Test	$V_{GS(Q)}$		-2.46		V

Functional Tests (In Test Fixture, 50 ohm system) : V_{DD} = 28 Vdc, I_{DQ} = 20 mA, f = 915MHz, Pulsed CW, 20uS/10%

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain@P1dB	Gp		20.4		dB
Drain Efficiency @ P_{SAT}	Eff		74.5		%
Saturated Power	P_{SAT}		41.9		dBm

Input Return Loss	IRL		-8		dB
Mismatch stress at all phases (Device no damage)	VSWR		10:1		Φ

TYPICAL CHARACTERISTICS

5.3-5.9GHz

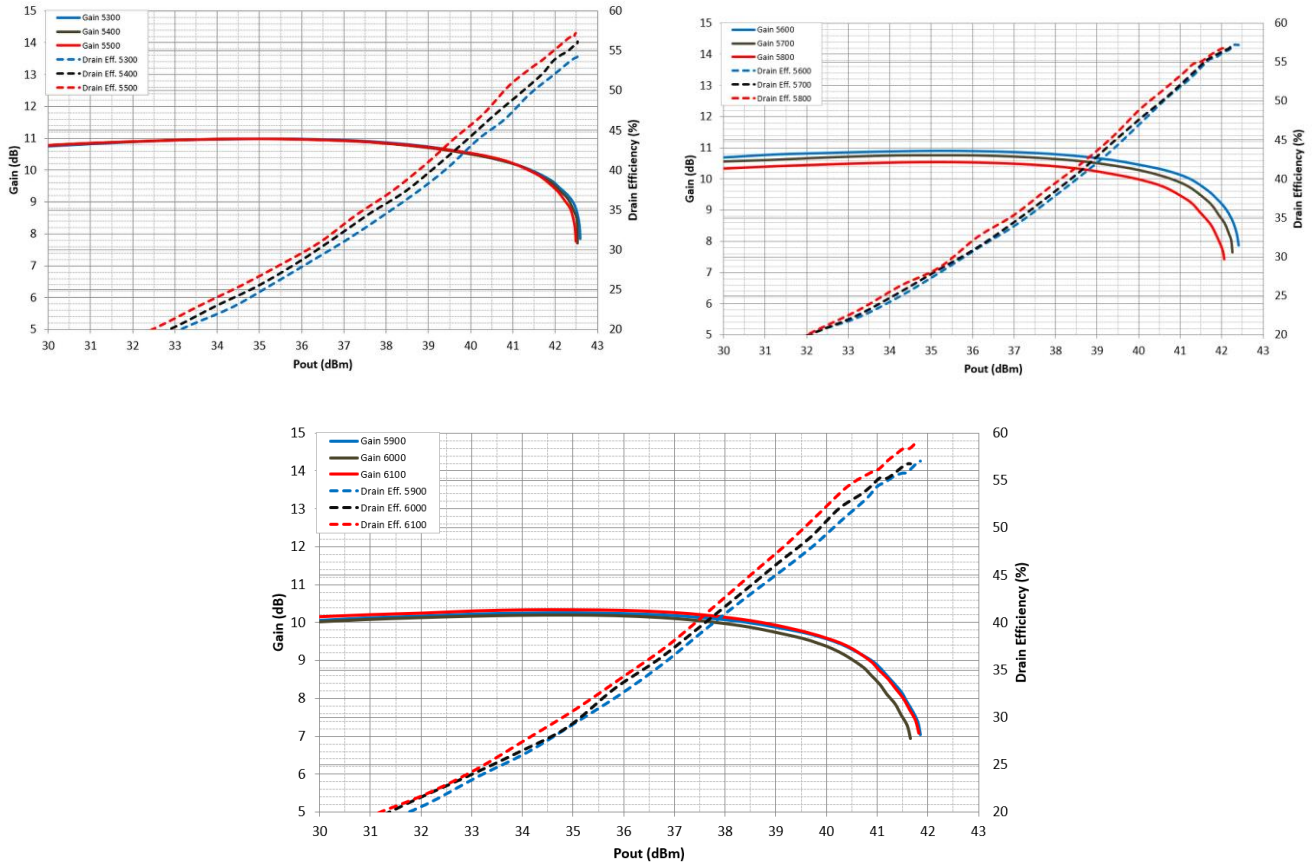


Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power

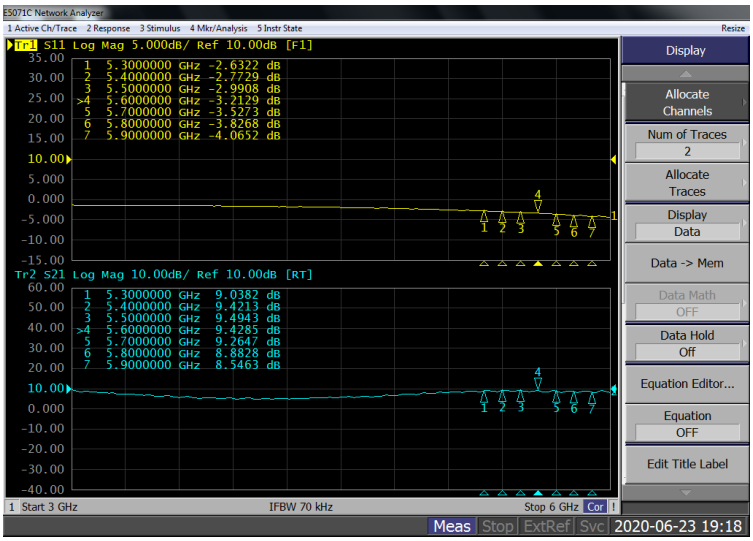
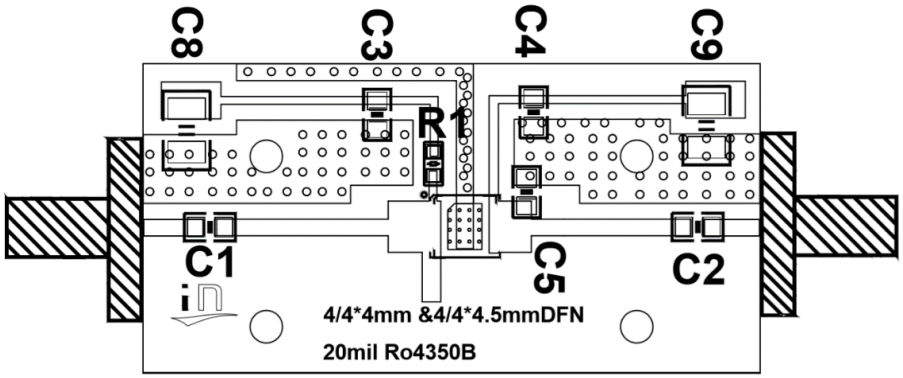


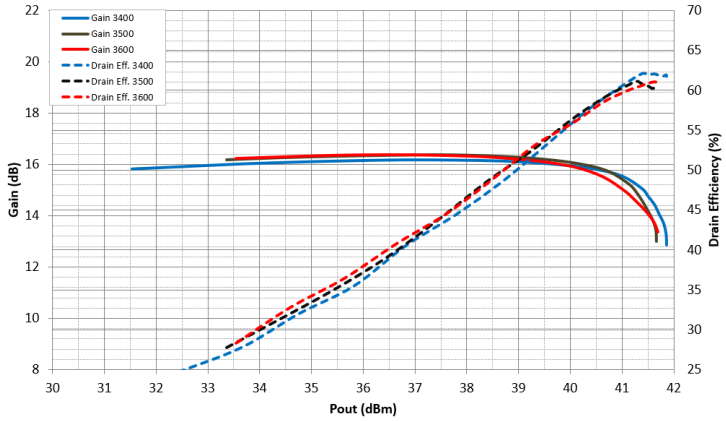
Figure 3. Network analyzer output S11/S21



BOM		
C1,C2,C3 C4	3.3pF	ATC600F
C5	0.4pF	ATC600F
C8,C9	10uF/63V	
R1	10 ohm	

Figure 5. PCB layout and bill of materials

3.4-3.8GHz



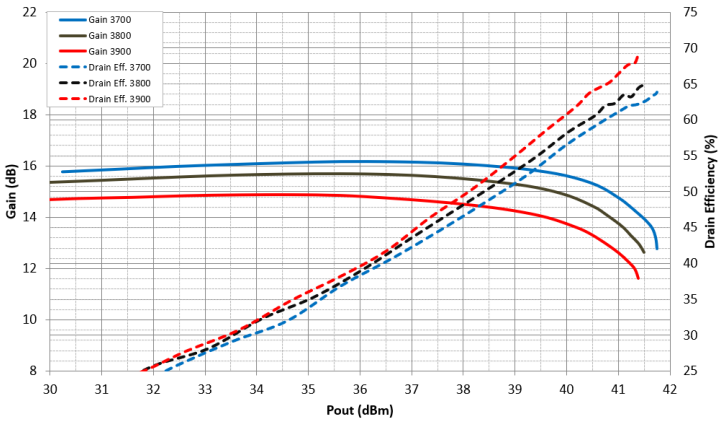


Figure 6. Power Gain and Drain Efficiency as Function of Pulse Output Power

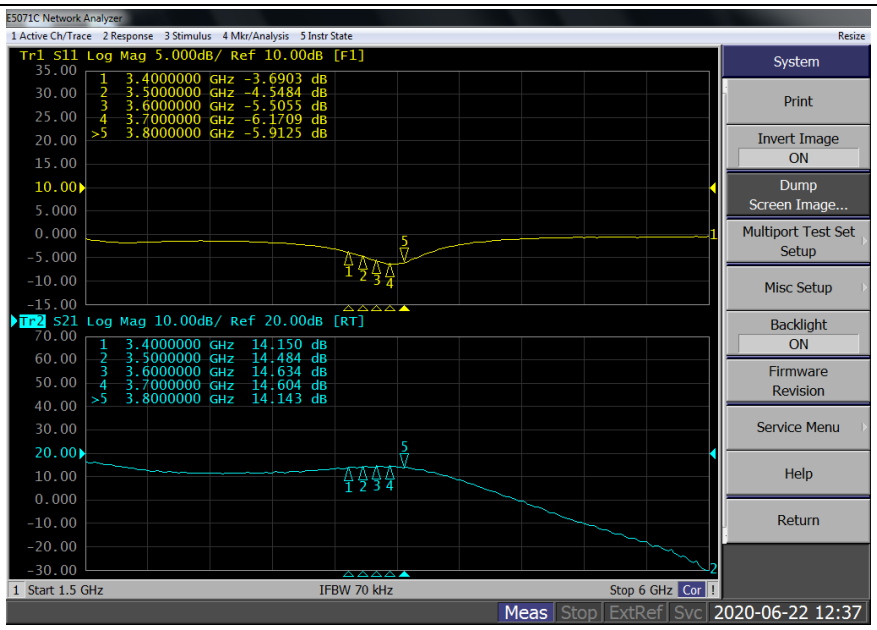
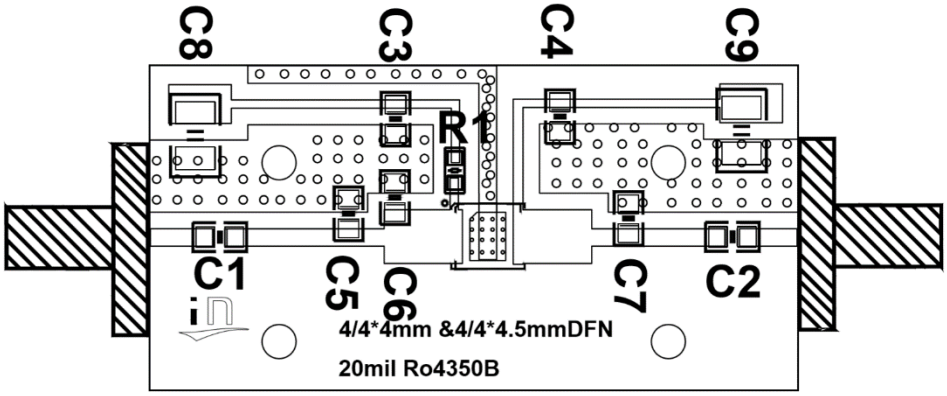


Figure 7. Network analyzer output S11/S21



BOM		
C1,C2,C3 C4	6.8pF	ATC600F
C5	0.2pF	ATC600F
C6，C7	1pF	ATC600F
C8,C9	10uF/63V	
R1	10 ohm	

Figure 8. PCB layout and bill of materials

2.3-2.7GHz

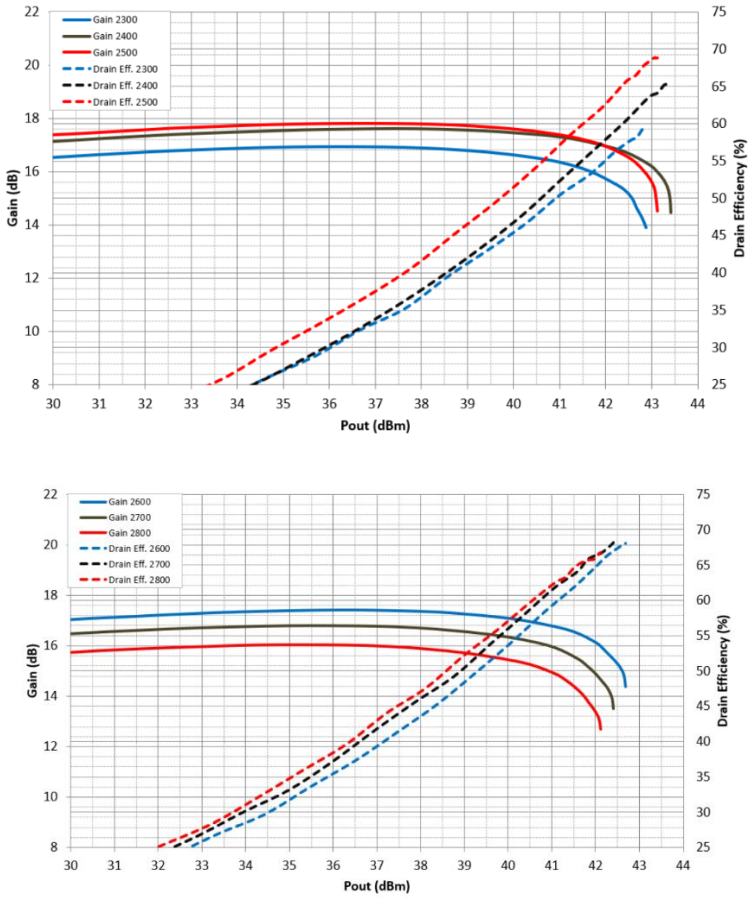


Figure 10. Power Gain and Drain Efficiency as Function of Pulse Output Power

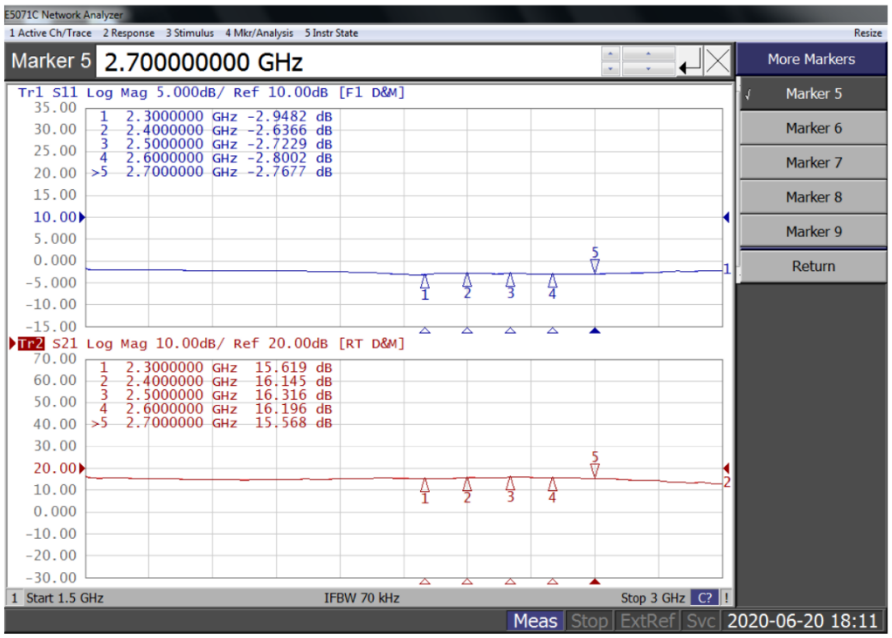
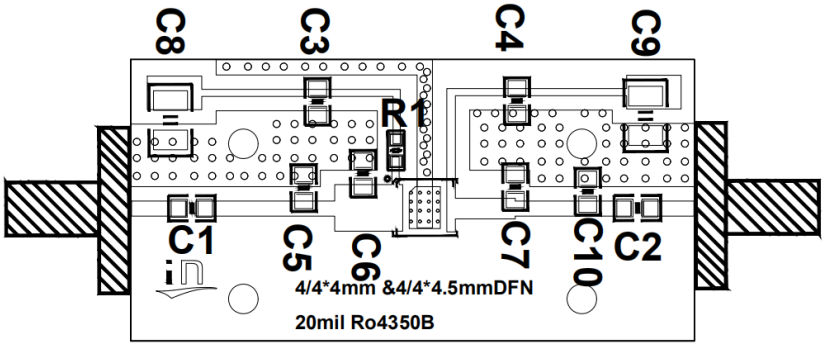


Figure 9. Network analyzer output S11/S21



BOM		
C1,C2,C3 C4	8.2pF	ATC600F
C5	1.5pF	ATC600F
C6，C7	1.0pF	ATC600F
C8,C9	10uF/63V	
C10	0.5pF	
R1	10 ohm	

Figure 10. PCB layout and bill of materials

1.2-2.2GHz

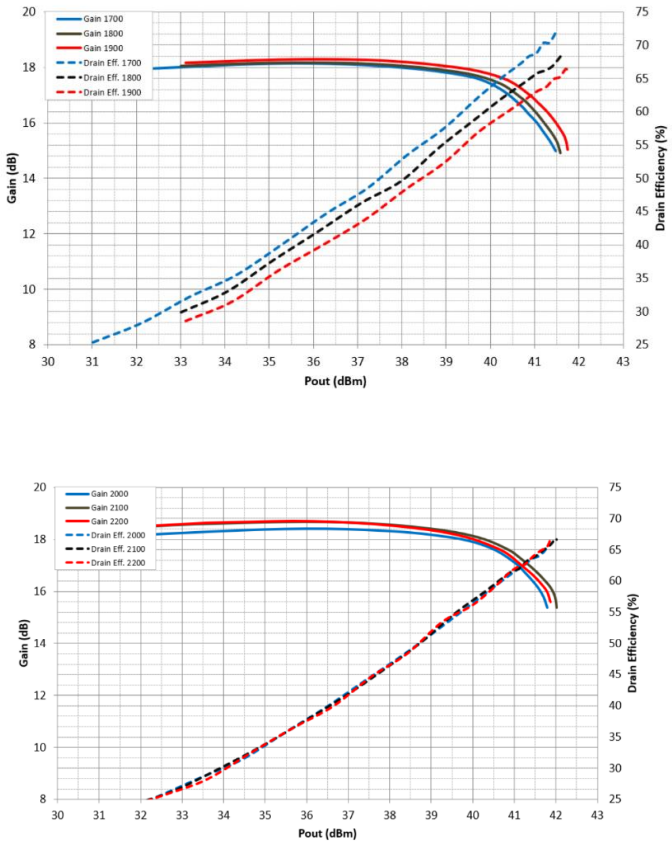


Figure 11. Power Gain and Drain Efficiency as Function of Pulse Output Power

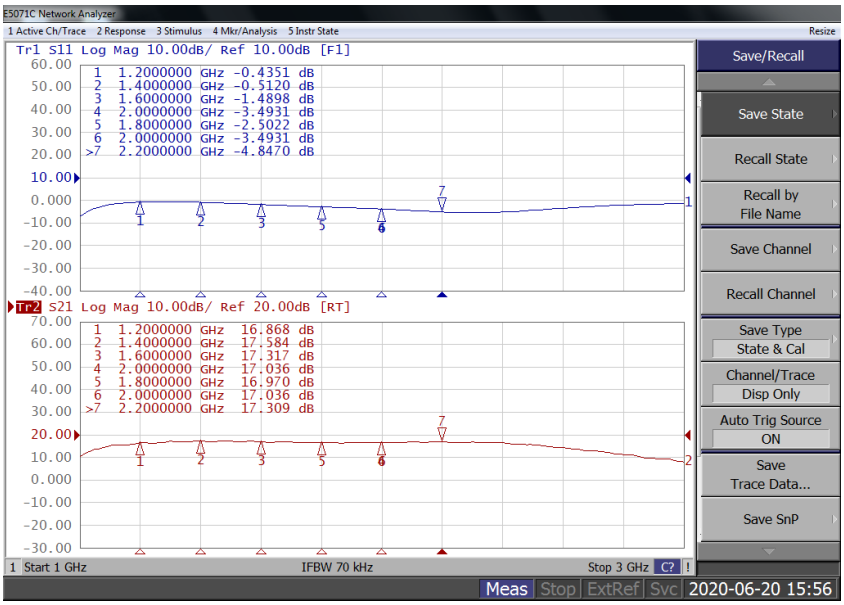
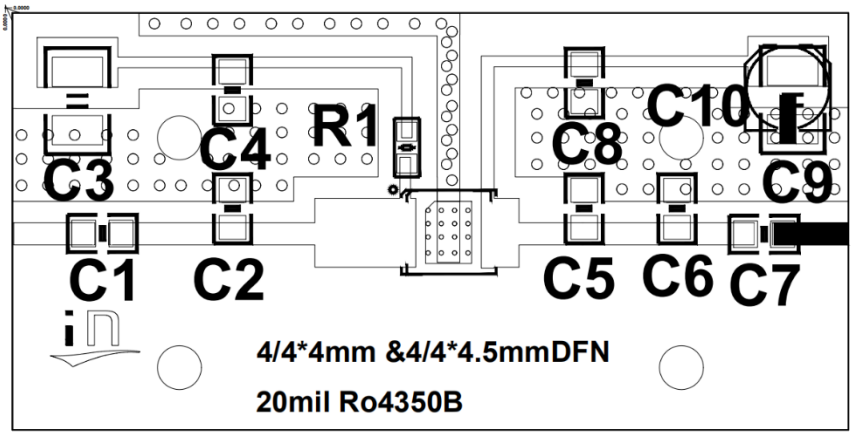


Figure 12. Network analyzer output S11/S21

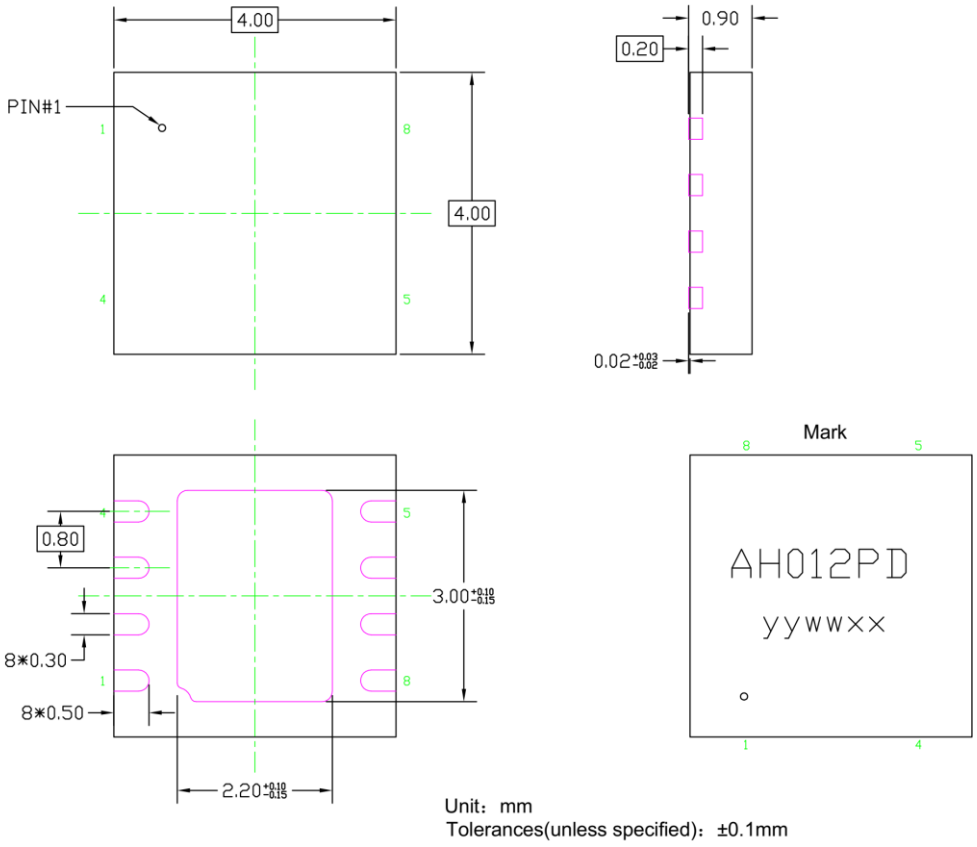


BOM		
C1,C4,C7,C8	12pF	ATC600F
C2	2pF	ATC600F
C5	0.4pF	ATC600F
C6	0.2pF	ATC600F
R1	10 ohm	
C10	470uF/63V	
C3,C9	10uF/63V	

Figure 1. PCB layout and bill of materials

Package Dimensions

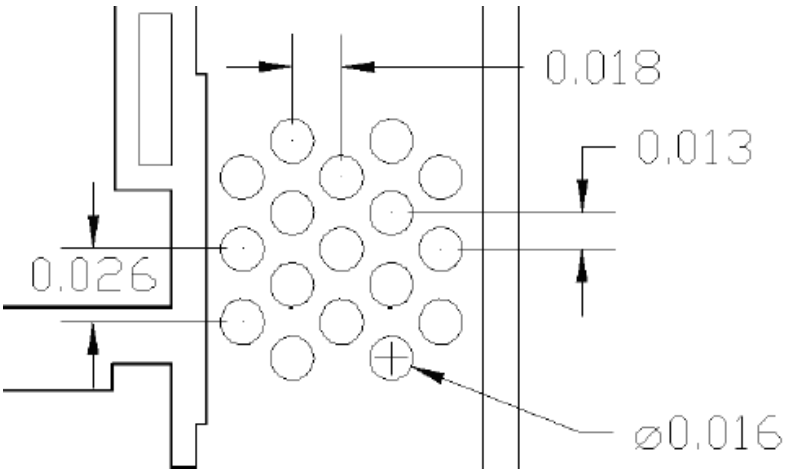
4*4 DFN Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.1mm.

Recommended vias layout: (all in inches)



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2019/11/27	V1.0	Objective Datasheet Creation
2019/11/29	V1.1	Pin definition modification
2020/6/28	V1.2	Add new application for multi bands

Application data based on ZYH-20-01,ZBB-20-14/15/16

Notice