Gallium Nitride 50V, 240W,2.5-2.7GHz RF Power Transistor

Description

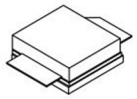
The STAV27240AY2 is a single ended 240watt, GaN HEMT, ideal for applications from 2.5 to 2.7GHz.

It is an input matched transistor capable of delivering Psat 270W.

It can support CW, pulse or any modulated signal.

There is no guarantee of performance when this part is used outside of stated frequencies.

STAV27240AY2



- Typical pulse CW performance across 2.5-2.7GHz

V_{DD} = 50 Vdc, I_{DQ} = 200mA, Pulse width=20us, duty cycle=20%, Tc=25°C

(On innogration application board with device soldered)

Freq(MHz)	P1(dBm)	P3(dBm)	P3(W)	Eff(%)@P3
2500	53.64	55.07	321	67.08
2600	53.00	54.54	284	68.75
2700	51.69	53.70	234	69.71

- WCMDA 3GPP TM1 64 DPCH 9.9 dB PAR @ 0.01% CCDF. VDS = 50 V, IDQ = 200 mA, POUT = 56W across 2.5-2.7G (On innogration Class AB application board with device soldered)

Freq(MHz)	Pout(dBm)	CCDF(dB	Ppeak(dBm)	Ppeak(W)	ACPR(dBc)	Gain(dB)	Efficiency(%)
2500	47.48	7.56	55.04	319.21	-36.71	16.75	33.86
2600	47.48	7.26	54.74	297.60	-34.74	17.11	37.10
2700	47.50	6.70	54.20	262.78	-32.59	17.02	41.05

Applications

- Sub-3GHz pulse or CW amplifier
- 5G N41 base station amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

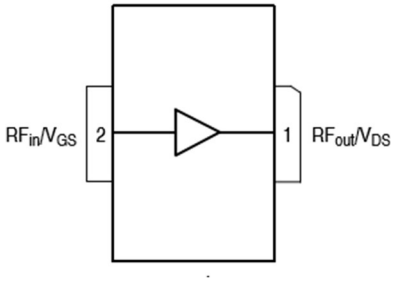


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	30	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=60W	$R_{\theta JC}$	1.4	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=30mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 30mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=200mA, Measured in Functional Test	$V_{GS(Q)}$		-3.23		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.6GHz, Pout=240W pulse CW for each path All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

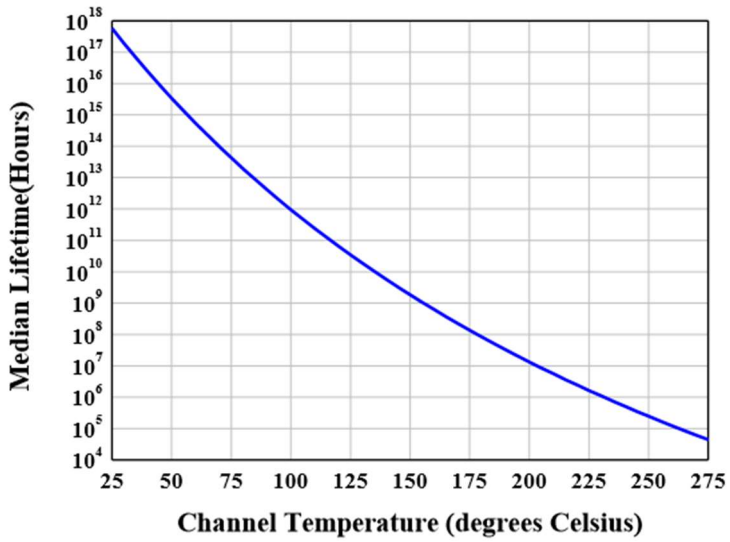
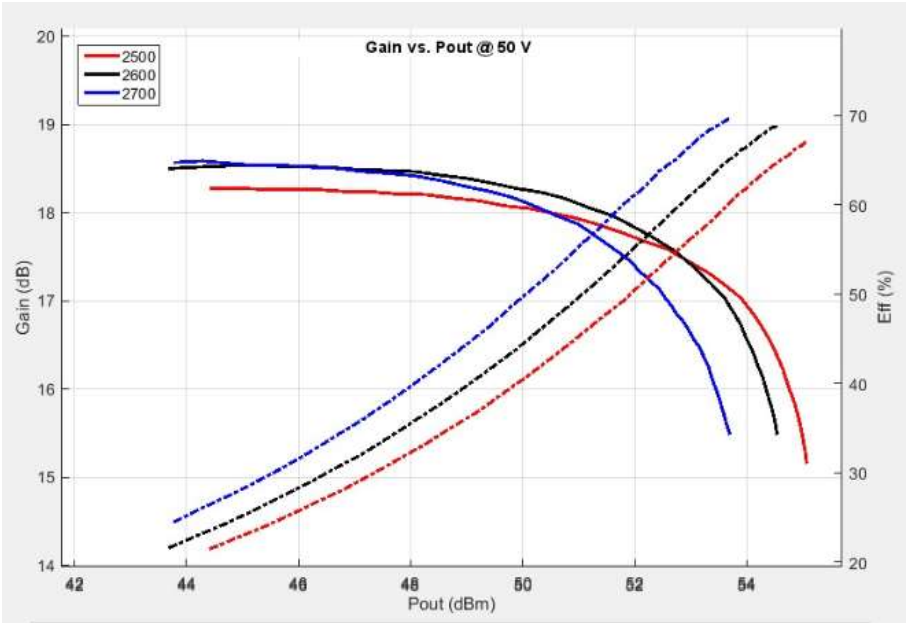


Figure 3: Efficiency and power gain as function of Pout

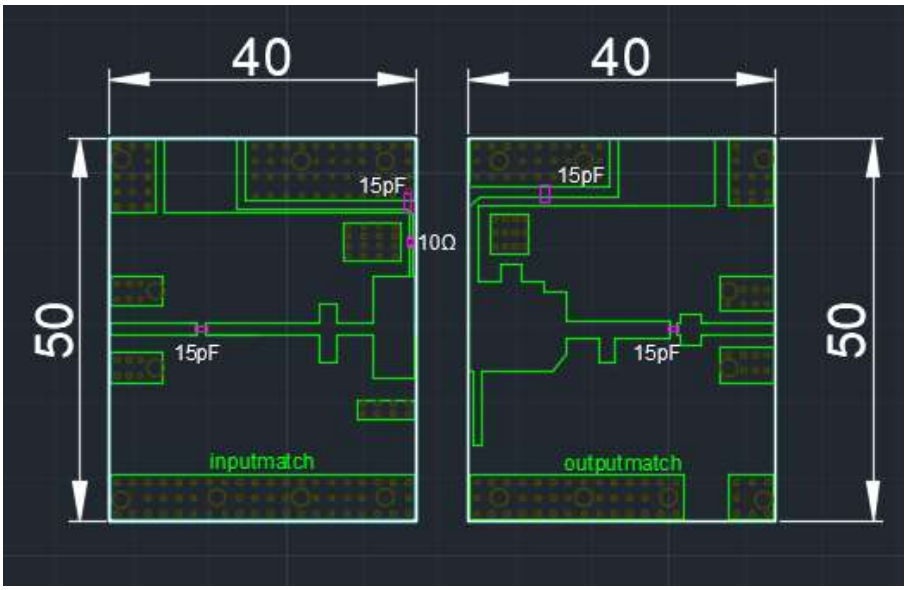
(VDD = 50Vdc, IDQ = 200 mA, Pulse width=20us, duty cycle=20%)



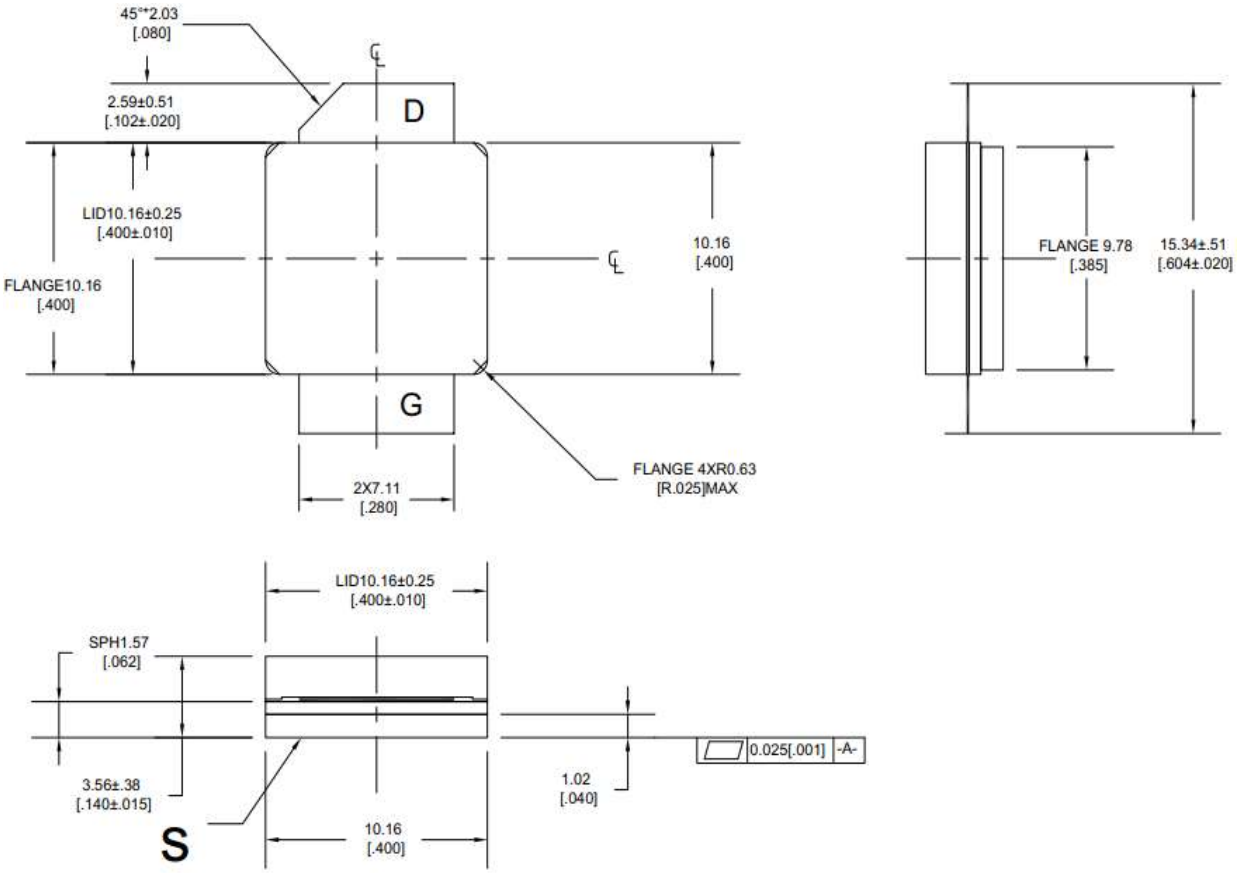
Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2500	53.64	231.41	59.97	17.16	55.07	321.04	67.08
2600	53.00	199.48	61.09	17.41	54.54	284.41	68.75
2700	51.69	147.59	59.34	17.56	53.70	234.19	69.71

Figure 4: S11 / S21 output from network analyzer

Figure 5: Picture of application board of 2.5-2.7GHz (RO4350B 30mils, PCB DXF file upon request)



Earless Flanged Ceramic Package; 2 leads



Unit: mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2020/4/14	**V1.0**	**Preliminary Datasheet Creation**

Application data based on: LWH-20-09

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