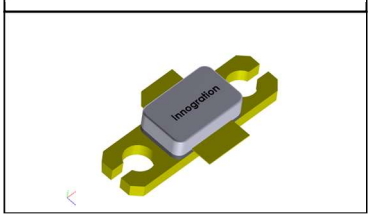
# SU6012V GaN TRANSISTOR

Document Number: SU6012V
Preliminary Datasheet V1.1

## Gallium Nitride 50V 115W, RF Power Transistor

**SU6012V**




### Description

The SU6012V is a 115W single ended, input matched GaN HEMT, designed for multiple applications with frequencies up to 3.7GHz.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical performance (on Innogration 2-3.7GHz class AB fixture with device soldered)

$V_{DD}$=50V $I_{DQ}$=100mA, Vgs=-3.04V

Pulse CW, pulse width: 20us, duty cycle: 10%

| Freq(MHz) | P1dB(dBm) | Gain(P1dB) | P3dB(W) | P3dB Eff(%) |
|---|---|---|---|---|
| 2000 | 49.89 | 12.06 | 137.02 | 57.55 |
| 2300 | 49.41 | 12.78 | 127.24 | 66.11 |
| 2600 | 50.68 | 12.21 | 154.12 | 64.85 |
| 2900 | 48.81 | 12.87 | 100.1 | 46.73 |
| 3200 | 49.65 | 13.09 | 119.38 | 44.72 |
| 3500 | 49.4 | 12.76 | 112.59 | 45.89 |

CW:

| Freq(MHz) | Pin(dBm) | Pout(W) | IDS(A) | Power Gain(dB) | Eff(%) |
|---|---|---|---|---|---|
| 2000 | 40.3 | 112.20 | 4.23 | 10.2 | 53.05 |
| 2100 | 40.1 | 120.23 | 4.14 | 10.7 | 58.08 |
| 2200 | 39.7 | 111.43 | 3.68 | 10.77 | 60.56 |
| 2300 | 39.5 | 104.71 | 3.6 | 10.7 | 58.17 |
| 2400 | 41.6 | 123.03 | 4.41 | 9.3 | 55.79 |
| 2500 | 40.47 | 112.20 | 4.38 | 10.03 | 51.23 |
| 2600 | 41 | 132.43 | 4.44 | 10.22 | 59.66 |
| 2700 | 40.6 | 117.49 | 4.09 | 10.1 | 57.45 |
| 2800 | 40.46 | 100.00 | 4.06 | 9.54 | 49.26 |
| 2900 | 40.1 | 87.70 | 4.21 | 9.33 | 41.66 |
| 3000 | 40 | 84.33 | 4.5 | 9.26 | 37.48 |
| 3100 | 40.26 | 87.10 | 4.7 | 9.14 | 37.06 |
| 3200 | 39.6 | 93.33 | 4.8 | 10.1 | 38.89 |
| 3300 | 40 | 100.00 | 4.74 | 10 | 42.19 |
| 3400 | 38.79 | 100.00 | 4.61 | 11.21 | 43.38 |
| 3500 | 40.2 | 91.20 | 4.6 | 9.4 | 39.65 |
| 3600 | 40.84 | 84.72 | 4.63 | 8.44 | 36.60 |
| 3700 | 41 | 81.85 | 4.75 | 8.13 | 34.46 |

### Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

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**Important Note: Proper Biasing Sequence for GaN HEMT Transistors**

**Turning the device ON**

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

**Turning the device OFF**

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain--Source Voltage | $V_{DSS}$ | +200 | Vdc |
| Gate--Source Voltage | $V_{GS}$ | -8 to 0 | Vdc |
| Operating Voltage | $V_{DD}$ | 0 to 55 | Vdc |
| Maximum forward gate current | Igf | 16 | mA |
| Storage Temperature Range | Tstg | -65 to +150 | C |
| Case Operating Temperature | $T_C$ | -55 to +150 | C |
| Operating Junction Temperature | $T_J$ | +225 | C |

**Table 2. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case<br>$T_C$= 85°C, $T_J$=200°C, DC Power Dissipation, FEA | $R_{\theta JC}$ | 2 | C/W |

**Table 3. Electrical Characteristics** ($T_C$ = 25℃ unless otherwise noted)

**DC Characteristics**

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $V_{GS}$=-8V; $I_{DS}$=16mA | $V_{DSS}$ | | 200 | | V |
| Gate Threshold Voltage | $V_{DS}$ = 50V, $I_D$ = 16mA | $V_{GS}$(th) | -4 | | -2 | V |
| Gate Quiescent Voltage | $V_{DS}$ =50V, $I_{DS}$=100mA, Measured in Functional Test | $V_{GS(Q)}$ | | -3.04 | | V |

## Reference Circuit of Test Fixture Assembly Diagram

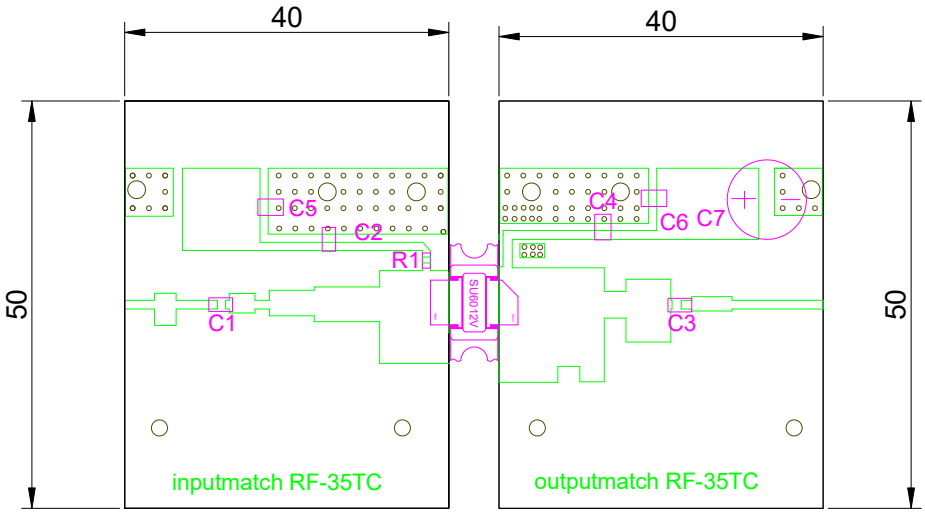



**Figure 1. Test Circuit Component Layout (2000-3700MHz)**

**Table 4. Test Circuit Component Designations and Values**

| Component | Description | Suggested Manufacturer |
|---|---|---|
| C1,C2,C3 | 9.1pF | DLC75D |
| C4 | 9.1PF | DLC70B |
| C5,C6 | Ceramic multilayer capacitor, 10uF, 100V | 10uF/100V |
| C7 | 470UF | 63V/470UF |
| R1 | Chip Resistor,15Ω,0805 | |
| PCB | 0.508mm [0.020"] thick, εr=3.5, RF-35TC, 1 oz. copper from Taconic | |

**Figure 2. Power Gain and Efficiency Vs frequency**

**Vgs = -3.04V, VDS= 50V, IDQ = 100mA, Pulsed CW, 20uS width, 10% dule cycle.**

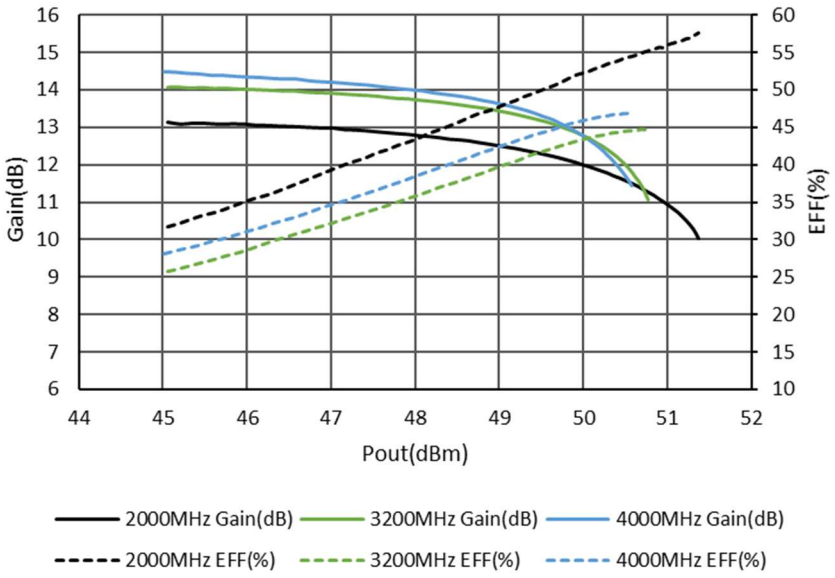
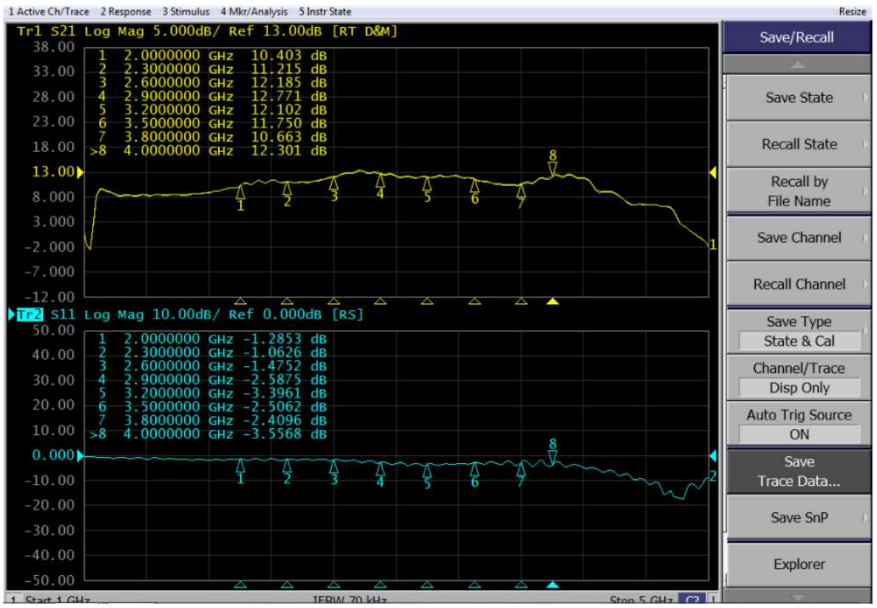
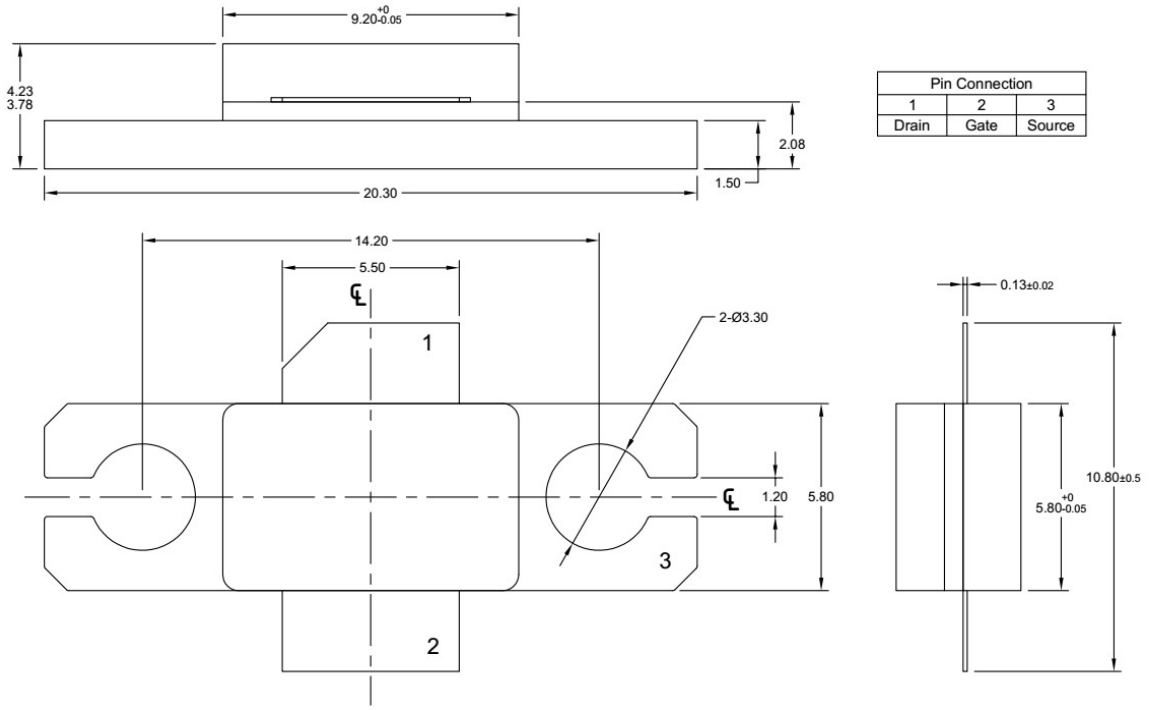



**Figure 3. Network Analyzer result S11 and S21 Vgs = -3.04V, VDS= 50V, IDQ = 100mA**



## Package Outline

### Flanged ceramic package; 2 leads




| OUTLINE VERSION | REFERENCE | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | |
| PKG-GXB | | | | | 10/10/2017 |

**Figure 1. Package Outline PKG-G2E**

## Revision history

**Table 4. Document revision history**

| Date | Revision | Datasheet Status |
|---|---|---|
| 2020/5/13 | V1.0 | Preliminary Datasheet creation |
| 2020/7/7 | V1.1 | Correct typo on 1st page |

**Application data based on YHG-20-11**

## Notice