

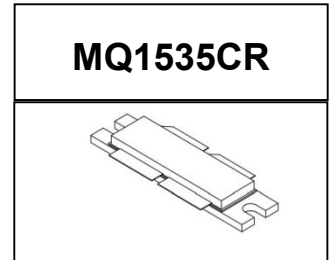
MQ1535CR LDMOS TRANSISTOR

Document Number: MQ1535CR
Preliminary Datasheet V1.0

350W, 28V High Power RF LDMOS FETs

Description

The MQ1535CR is a 350-watt capable, high performance, unmatched push pull LDMOS FET, for wide-band commercial and industrial applications with frequencies 200 to 700MHz. It can be used for both CW and pulse application or any other modulation signal. It is featured for high power and high ruggedness, low thermal resistor, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and mobile radio applications.



- Typical Performance at 28V and 30V (On Innogration 200-512MHz wideband fixture with device soldered):

MQ1535CR VDS=28V, VGS=2.67V, IDQ=150mA CW						
Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
200	37.62	53.71	235.0	14	16.09	59.94
300	37.91	53.55	226.5	11.89	15.64	68.02
400	39.37	53.97	249.5	15.4	14.6	57.85
512	39.55	54.1	257.0	16.6	14.55	55.30

MQ1535CR VDS=30V, VGS=2.67V, IDQ=150mA CW						
Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
200	38.61	54.37	273.5	15.7	15.76	58.07
300	37.91	54.01	251.8	12.35	16.1	67.95
400	39.37	54.38	274.2	15.9	15.01	57.48
512	39.55	54.39	274.8	17.4	14.84	52.64

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCl dri
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 225-512MHz (ultra shortwave communication)
- 470-700MHz (TV UHF)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C

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Operating Junction Temperature	T_j	+225	°C
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Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.15	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 1.0\text{mA}$	$V_{(BR)DSS}$	65			V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}$, $I_D = 800\ \mu\text{A}$)	$V_{GS(th)}$	—	2.2	—	V
Gate Quiescent Voltage ($V_{DD} = 28\text{V}$, $I_D = 150\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.67	—	V
Common Source Input Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{ISS}		140		pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{OSS}		60		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{RSS}		2.2		pF

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Reference Circuit of Test Fixture Assembly Diagram (Layout file upon request, 30mil RO4350)

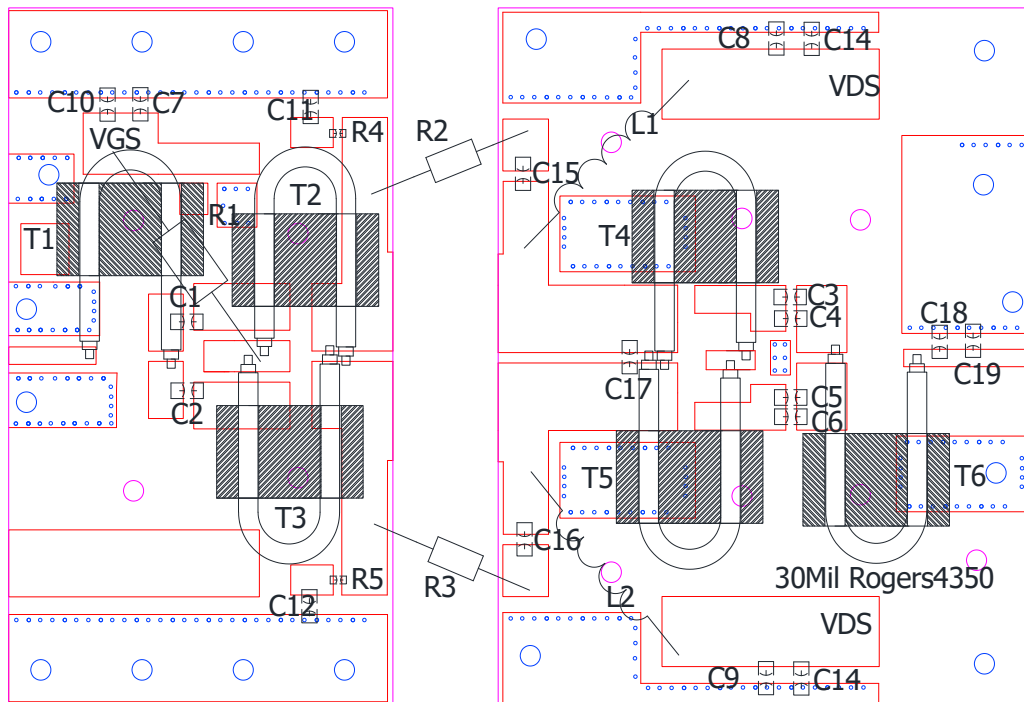


Table 5. Test Circuit Component Designations and Values

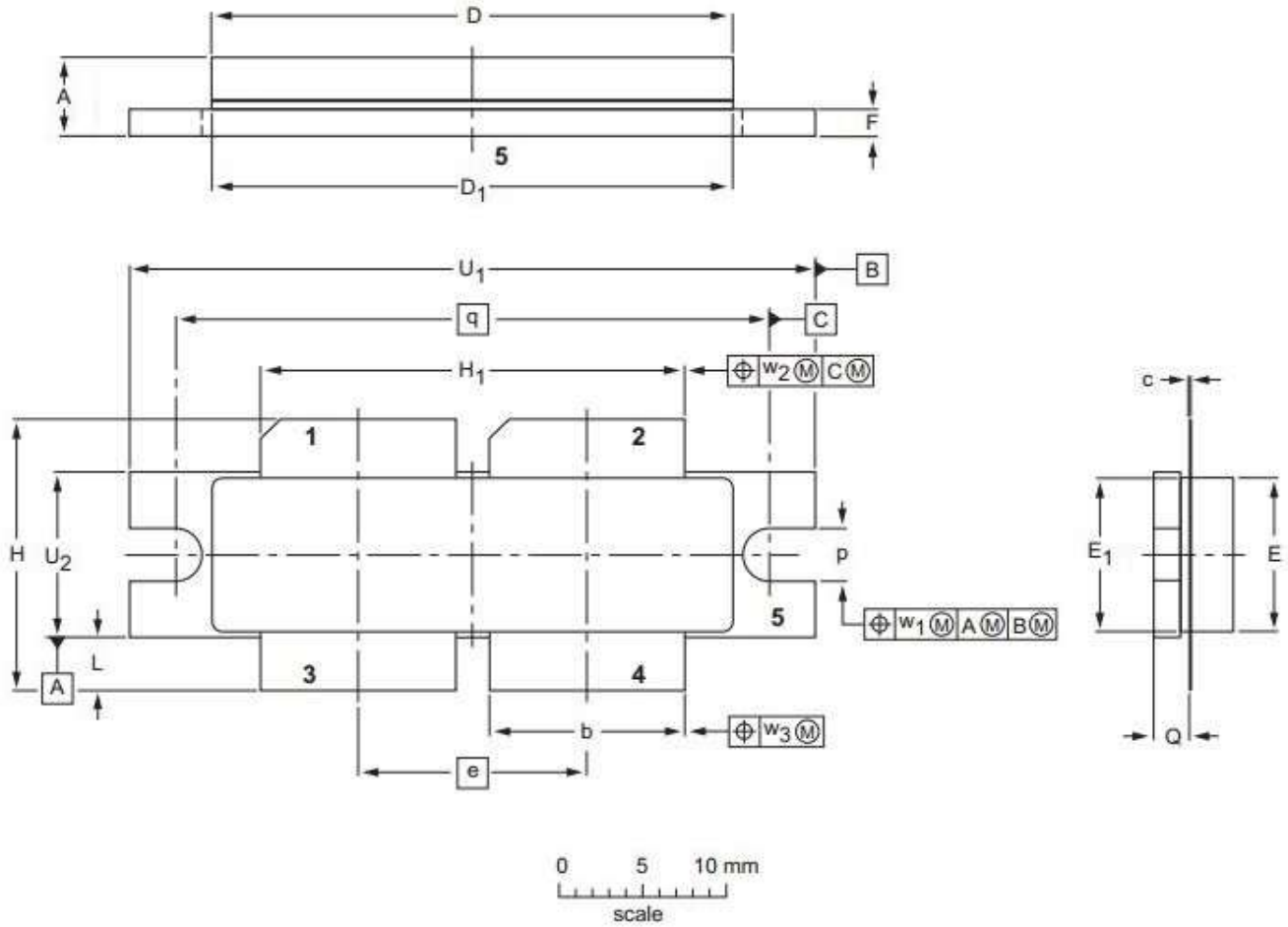
Component	Description	Suggested Manufacturer
C1~C9	470pF	DLC70B
C10~C14	10uF	Ceramic multilayer capacitor
C15,C16	10nF	Ceramic multilayer capacitor
C17	8.2pF	DLC70B
C18	1.2pF	DLC70B
C19	1.5pF	DLC70B
R1	235ohm	
R2,R3	270ohm	3W/270ohm
R4,R5	11 Ω	0805
T1,T6	50ohm, Line length=70mm	SF-086-50
T2,T3,T4,T5	12.5ohm, Line length=70mm	SFF-12.5-1.5
L1,L2	10 turns 线径 0.8mm, 绕径 3mm	

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1, 2—DRAIN, 3, 4—GATE, 5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₃
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/11/18	Rev 1.0	Preliminary Datasheet

Application data based on HL-21-42

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