



## Gallium Nitride 28V 4W, General purpose RF Power Transistor

### Description

The GTAH80004PD is a 4W GaN HEMT, designed for multiple applications, up to 8000MHz.

The transistor is available in a highly cost effective 4mm\*4mm, surface mount, DFN package with 100% DC production test to ensure the quality and consistency.

It can be used in CW, Pulse and any other modulation modes, especially LTE-U/WIFI 6/WIFI 6E etc.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical Performance of class AB circuit (On Innegration fixture):

$V_{DD} = 32\text{ V}$ ,  $I_{DQ} = 10\text{ mA}$ , CW,

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	Eff(%)
7200	28	36.94	4.9	0.0333	8.94	46.39
7300	26.64	36.64	4.6	0.0318	10	45.33
7400	26.5	36.99	5.0	0.0333	10.49	46.93
7500	26.28	37.08	5.1	0.0339	10.8	47.06
7600	26.5	37.1	5.1	0.0339	10.6	47.28
7700	27.41	36.91	4.9	0.033	9.5	46.49
7800	27.95	36.82	4.8	0.0305	8.87	49.27

Other application data available upon request: 1.8-2.2GHz, 2.3-2.7, 3.4-3.8GHz

### Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

### Note: Proper Biasing Sequence for GaN HEMT Transistors

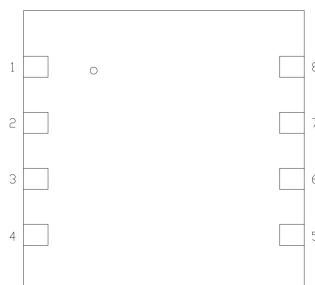
#### Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage (28V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

### Pin Configuration and Description(Top view)



### GTAH80004PD



DFN 4\*4mm



Pin No.	Symbol	Description
2, 3	RF IN /VGS	RF Input, Gate Bias
6, 7	RF OUT /MDS	RF Output, Drain Bias
1, 4, 5, 8	NC	No connection
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

**Table 1. Maximum Ratings (Not simultaneous, TC = 25°C unless otherwise noted)**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	150	Vdc
Gate--Source Voltage	$V_{GS}$	-10,+2	Vdc
Operating Voltage	$V_{DD}$	40	Vdc
Maximum Forward Gate Current	$I_{gmax}$	1	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	+150	°C
Operating Junction Temperature(See note 1)	$T_J$	+225	°C

1. Continuous operation at maximum junction temperature will affect MTTF
2. Bias Conditions should also satisfy the following expression:  $P_{diss} < (T_j - T_c) / R_{JC}$  and  $T_c = T_{case}$

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$ , $T_J = 200^\circ\text{C}$ , DC Power Dissipation, FEA (See note 1)	$R_{\theta JC-DC}$	16	C/W

1.  $R_{\theta JC-DC}$  is tested at only DC condition, it is related to the highest thermal resistor value among all test conditions. It might be differently lower in different RF operation conditions like CW signal ,pulsed RF signal etc.

**Table 3. Electrical Characteristics ( $T_C = 25^\circ\text{C}$  unless otherwise noted)**

**DC Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ ; $I_{DS} = 1\text{mA}$	$V_{DSS}$		150		V
Gate Threshold Voltage	$V_{DS} = 28\text{V}$ , $I_D = 1\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 32\text{V}$ , $I_{DS} = 10\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$	---	-2.4	---	V

**Functional Tests (In Innegration broadband Test Fixture, 50 ohm system) :  $V_{DD} = 32\text{Vdc}$ ,  $I_{DQ} = 10\text{mA}$ ,  $f = 7500\text{MHz}$ , CW**

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @Psat	$G_p$	8			dB
Drain Efficiency @Psat	$Eff$	45	49		%
Saturated Power	$P_{sat}$	4	5		W
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases(No device damage)	VSWR		10:1		Ψ

## TYPICAL CHARACTERISTICS

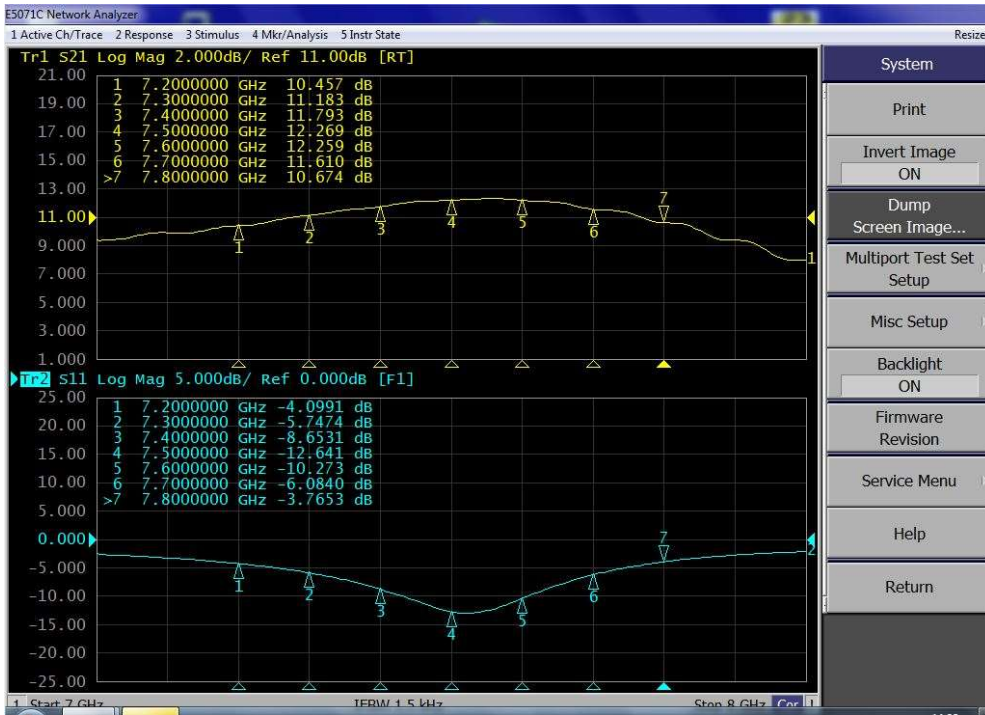


Figure 1. Network analyzer output S11/S21

### Reference circuit of test fixture assembly diagram

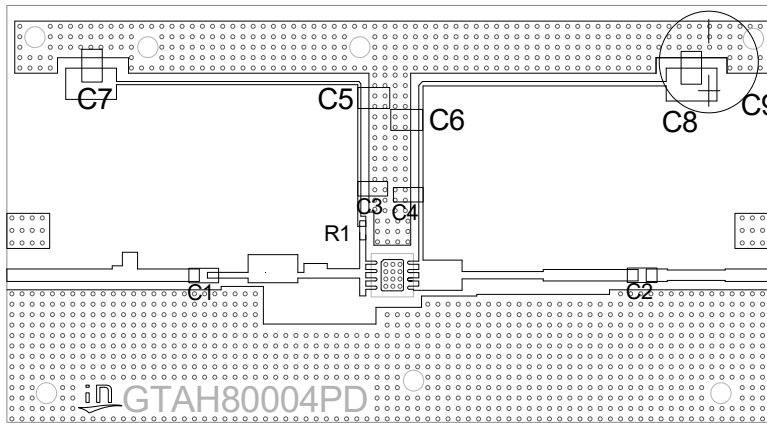


Figure 5. 7200-7800MHz fixture

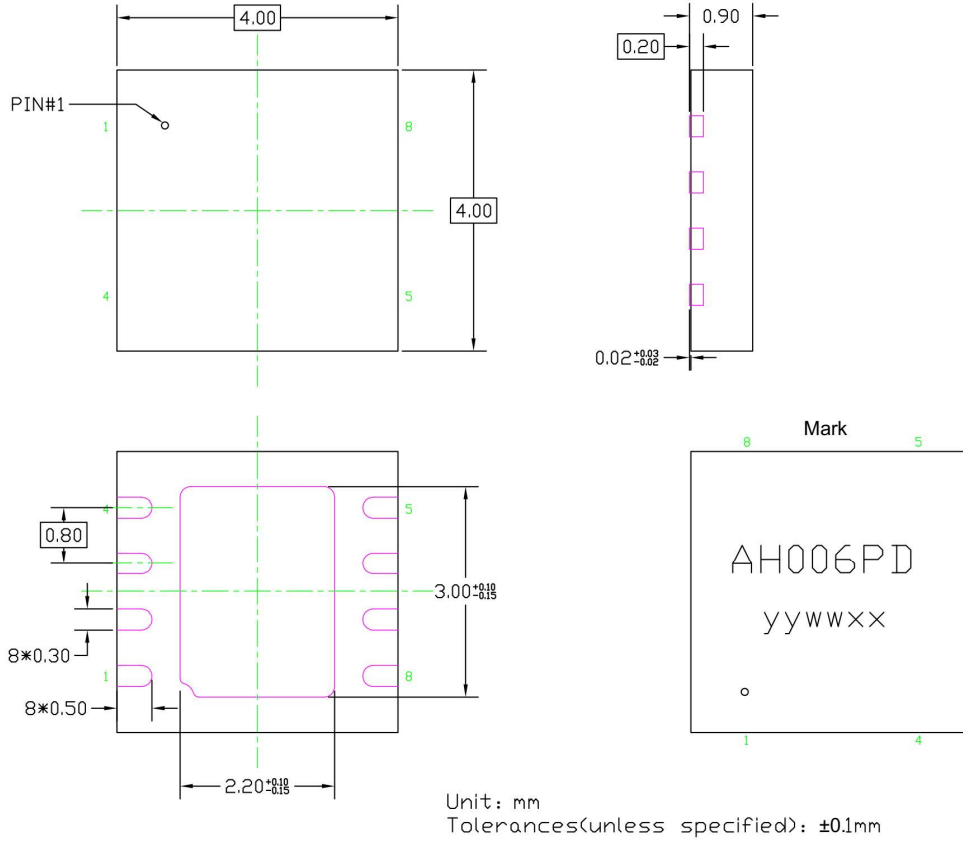
Table 4: components designations and values of 7200-7800Mhz fixture

Component	Description	Suggested Manufacturer
C1、C2、C3、C4	1.8pF	DLC75D
C5、C6、C7、C8	Ceramic multilayer capacitor, 10uF, 100V	10uF/100V
C9	470UF	63V/470UF
R1	Chip Resistor, 11 Ω, 0603	
PCB	0.508mm [0.020"] thick, εr=3.5, Rogers 4350B	



### Package Dimensions

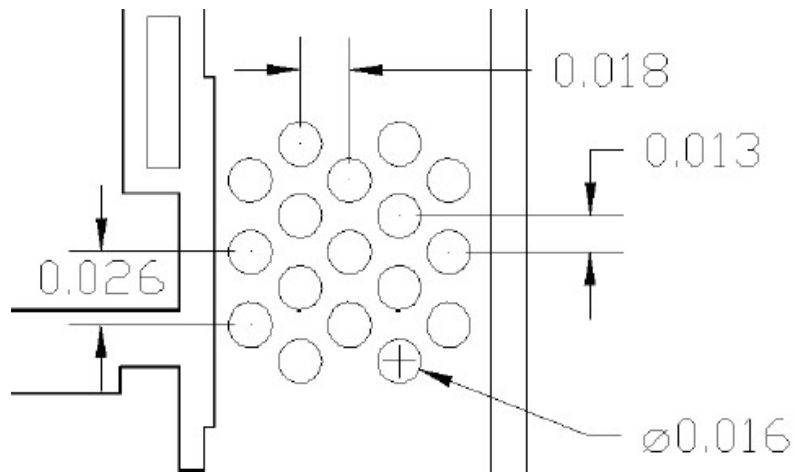
#### 4\*4 DFN Package



#### Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are  $\pm 0.1\text{mm}$ .

#### Recommended vias layout: (all in inches)





## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2021/4/20	V1.0	Preliminary Datasheet Creation
2021/11/3	V1.1	1.8-2.2,2.3-2.7,3.4-3.8GHz data ready

Application data based on YHG-21-10/ZXY

### Notice

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