MU0517VX LDMOS TRANSISTOR

Document Number: MU0517VX
Preliminary Datasheet V1.0

170W, 50V High Power RF LDMOS FETs

MU0517VX

Description

The MU0517VX is a 170-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.5 GHz.

It is featured by single ended configuration for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical performance(on Innogration test board with device soldered)

  Signal: CW , Vgs=3.4v,Vds=50v,Idq=180mA

Freq (MHz)	Pin (dBm)	Psat (dBm)	Psat (W)	IDS (A)	Gain (dB)	Eff (%)	2nd harmonic (dBc)	3rd harmonic (dBc)
123	27.8	52.15	164.1	4.22	24.35	78	-26	-35
128	27.7	51.99	158.1	3.98	24.29	79	-26	-36
133	28.6	51.47	140.3	3.53	22.87	79	-26	-37

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 180 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.4	——	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)				mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}				pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}				pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}				pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f =160MHz, pulse width:100us, duty cycle:10%

Load 20:1 All phase angles, at 250W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout at 128MHz

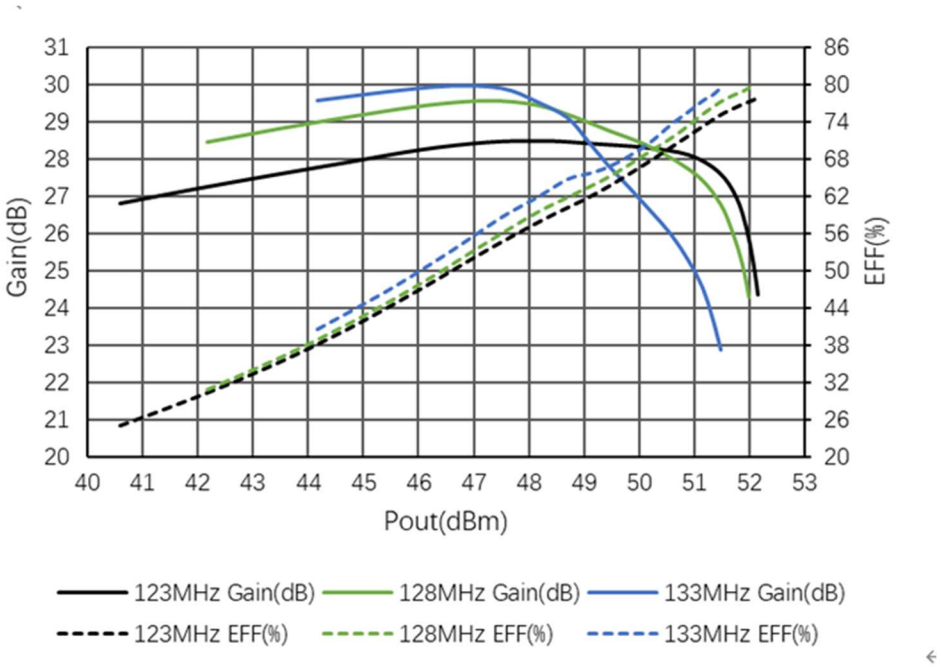


Figure 1: Network analyzer output S11/221

Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)

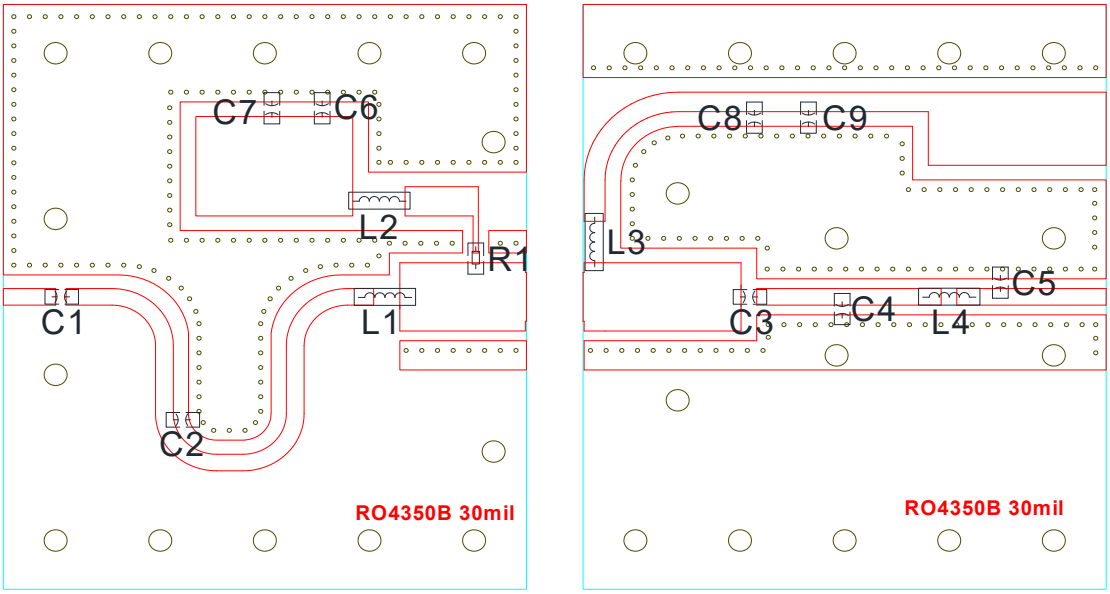
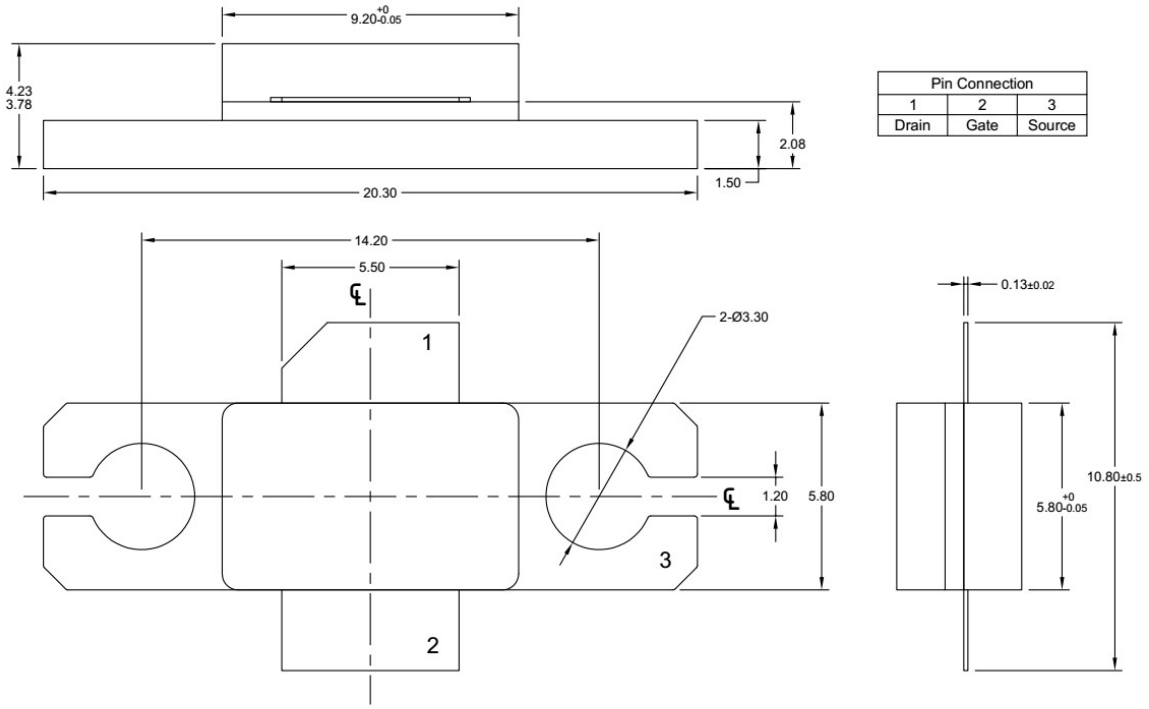


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1,C6,C8	1000pF	DLC70B
C2	100pF	DLC70B
C3	200pF	ATC800B
C4	30pF	DLC70B
C5	47pF	ATC800B
C7,C9	10uF	10uF/50V
R1	Chip Resistor,9.1Ω,	1206
L1	10nH	1606
L2,L3,L4	34nH,4turns	线径 1mm, 绕径 3.5mm

Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/5/29	Rev 1.0	Preliminary Datasheet Creation

Application data based on HL-21-01/02

Disclaimers