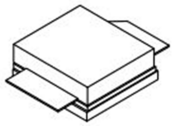
MG3107AS LDMOS TRANSISTOR

Document Number: MG3107AS
Product Datasheet V1.0

70W, S band High Power RF LDMOS FETs

MG3107AS



Description

The MG3107AS is a 70-watt, internally matched, single ended LDMOS FETs, designed for multiple applications within 2.7-3.1GHz. It can be used in Class AB/B and Class C for all typical modulation formats. Within narrower band like 2.7-2.9GHz, it can be used as 90W.

- Typical Performance (On Innogration fixture with device soldered):
  V_{DD} = 32 Volts, I_{DQ} = 50 mA, CW.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2800	49.52	89.5	45.8	10.36	50.17	103.9	46.5
2900	49.58	90.8	46.0	10.98	50.27	106.5	46.8
3000	49.01	79.6	45.7	11.31	49.77	94.9	46.7
3100	48.14	65.2	45.0	11.2	48.86	77.0	45.0

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- S band pulse amplifier
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.9	°C/W

Table 3. ESD Protection Characteristics

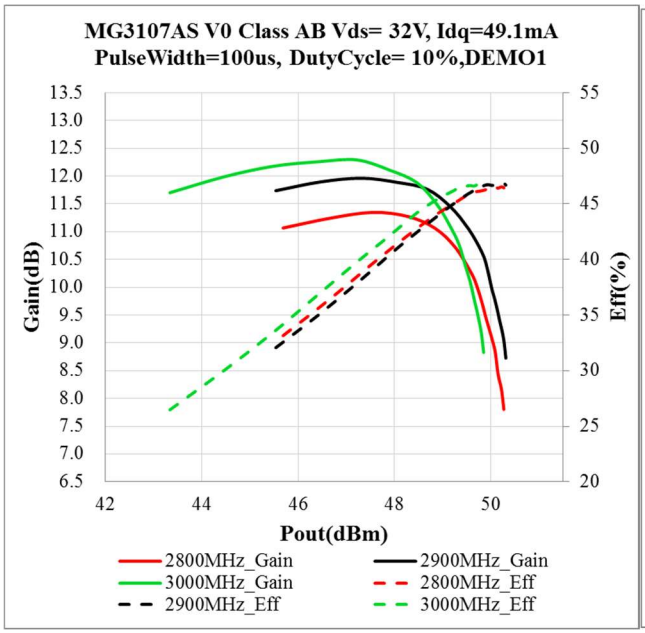
Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 450 μA)	$V_{GS(th)}$		2.0		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 380 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.1		V
Functional Tests (On Demo Test Fixture, 50 ohm system) V_{DD} = 32 Vdc, I_{DQ} = 50 mA, f = 3100 MHz, Pulse CW Signal Measurements.					
Power Gain	Gp		9		dB
Drain Efficiency@P1dB	η_D		45		%
3 dB Compression Point	P_{-3dB}	70			W
Input Return Loss	IRL		-10		dB
Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 32 Vdc, I_{DQ} = 50 mA, f = 3100 MHz					
VSWR 10:1 at 70W pulse CW Output Power	No Device Degradation				

TYPICAL CHARACTERISTICS

Figure 1. Power Gain and Drain Efficiency as Function of Pulse Output Power



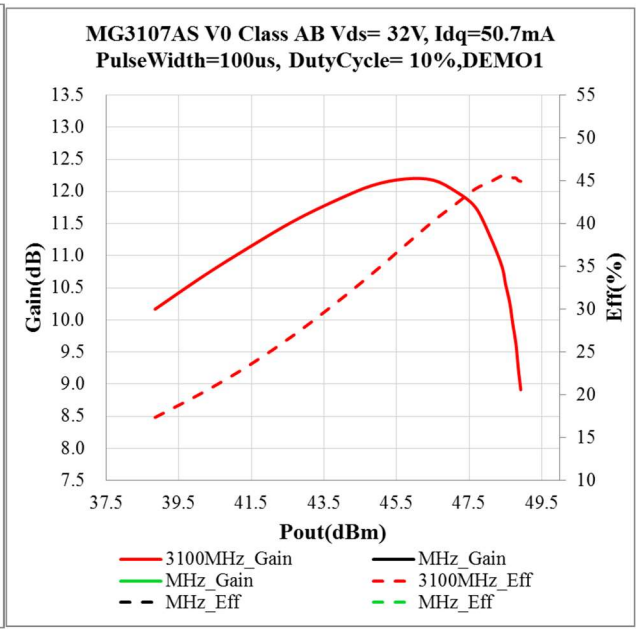


Figure 2. Network analyzer output S11/S21 (VDS=32V IDQ=380mA VGS=3.1V)

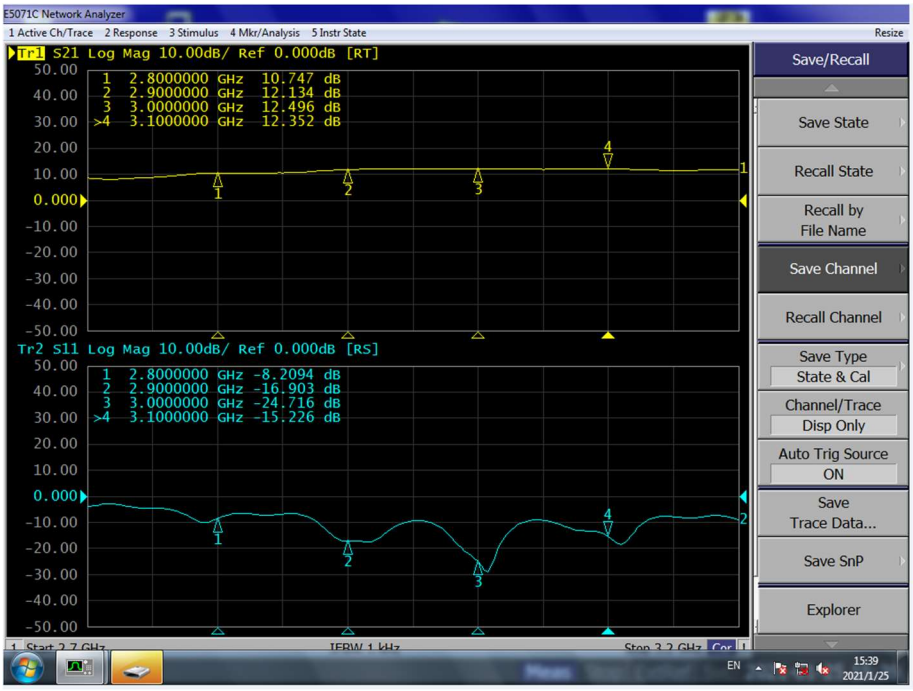


Figure 3. Test Circuit Component Layout

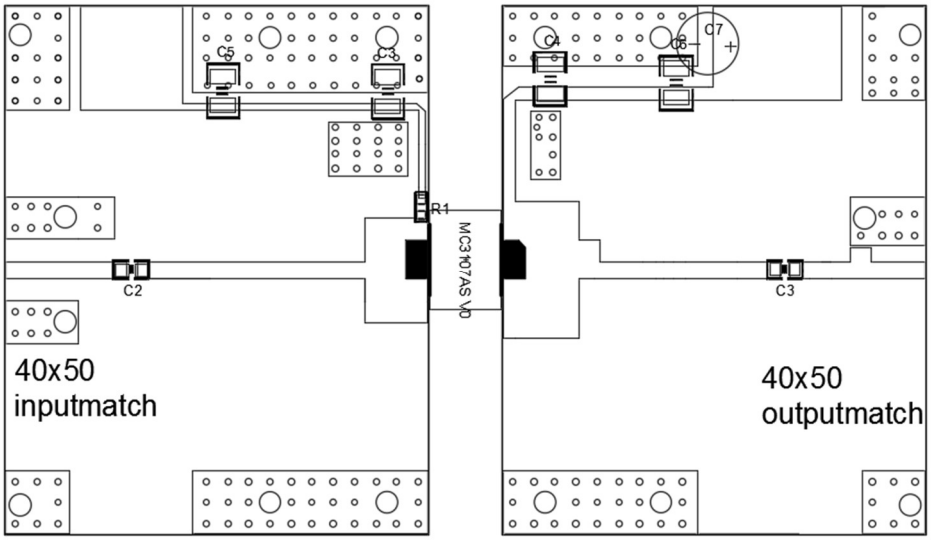
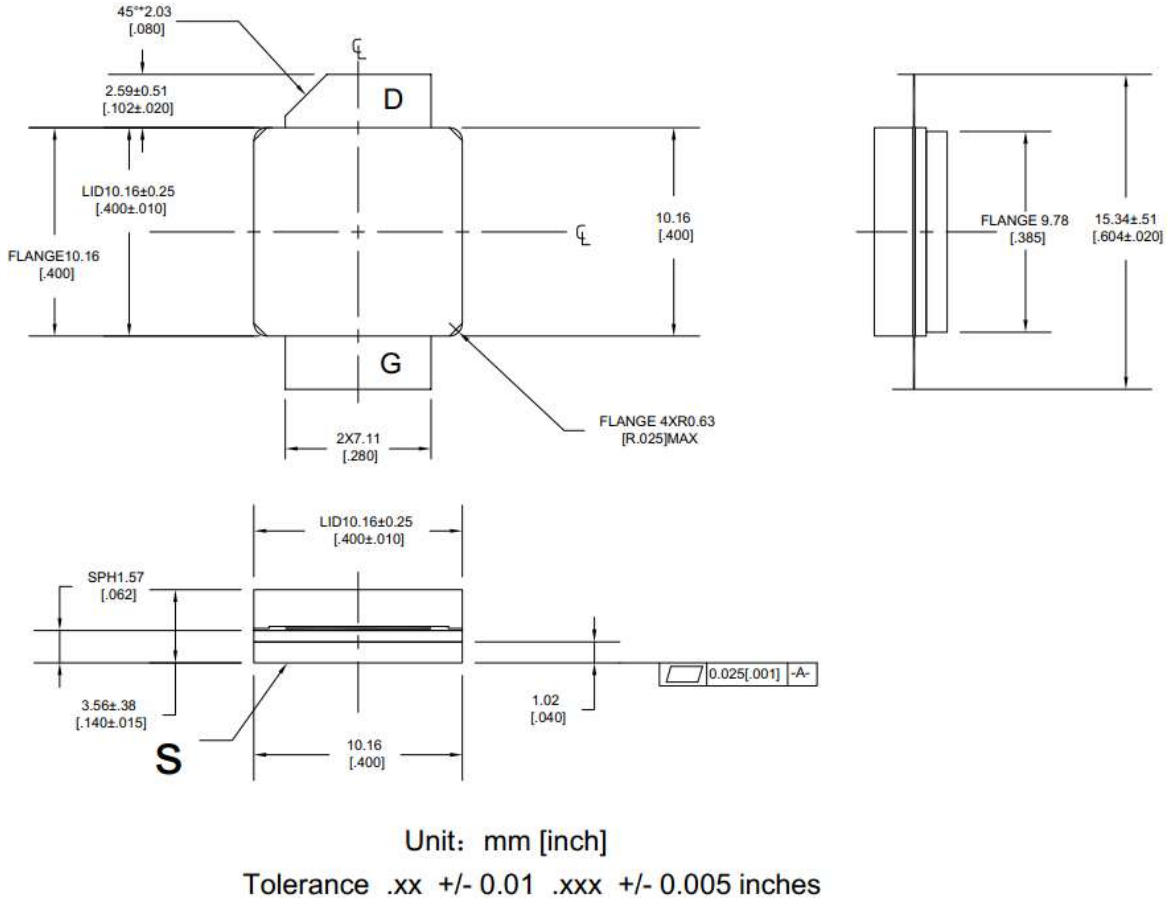


Table 4. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C2,C3,C4	12pF	DLC75D
C5 C6	Ceramic multilayer capacitor, 10uF, 100V	DLC75D
R1	Chip Resistor,9.1 Ω	
C7	470UF 63V	
PCB	0.762mm [0.030"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper	

Package Outline

Earless flanged ceramic package; 2 leads



Unit: mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/1/26	**Rev 1.0**	**Product Datasheet**

Application data based on HL-21-03

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