Gallium Nitride 28V 6W, General purpose RF Power Transistor

Description

The GTAH35006PD is a 6W GaN HEMT, designed for multiple applications, up to 6000MHz. The transistor is available in a highly cost effective 4mm*4mm, surface mount, DFN package with 100% DC production test to ensure the quality and consistency.

It can be used in CW, Pulse and any other modulation modes.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

GTAH35006PD

DFN 4*4mm

- Typical Performance of class AB circuit (On Innogration fixture):

V_{DD} =28 V, I_{DQ} =30 mA, Pulse CW, Pulse Width=20 us, Duty cycle=10%.

Freq (GHz)	Pulse CW Signal				
	P1dB (dBm)	Gain@ P1dB (dB)	P3dB (dBm)	Eff@P3 (%)	Note
2.5	39.17	18.7	39.94	62.7	Fixture 1
2.6	39.27	18.8	39.78	64.5	
2.7	39.13	18.9	39.67	63.6	
3.4	39.0	17.5	39.8	65.0	Fixture 2
3.5	38.7	18.4	39.5	66.6	
3.6	38.2	18.2	39.3	67.2	
4.8	38.56	15.0	39.36	61.4	Fixture 3
4.9	38.46	15.2	39.30	61.5	
5	38.10	15.1	39.18	61.7	
5.7	38.74	12.6	39.86	60.4	Fixture 4
5.8	38.60	13.0	39.65	60.0	
5.9	38.16	12.7	39.50	62.2	

- Other available fixtures: 1.8-2.2GHz, 0.7-1GHz, 2-4GHz，
- All fixtures reuse the same basic PCB with slightly different layout or bill of materials

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

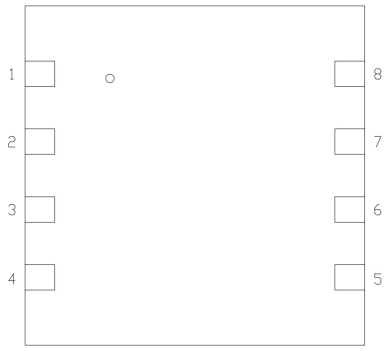
Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (28V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
2, 3	RF IN /VGS	RF Input, Gate Bias
6, 7	RF OUT /VDS	RF Output, Drain Bias
1, 4, 5, 8	NC	No connection
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	125	Vdc
Gate--Source Voltage	V_{GS}	-10,+2	Vdc
Operating Voltage	V_{DD}	40	Vdc
Maximum Forward Gate Current @ TC = 25°C	Igmax	1.5	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature(See note 1)	T_J	+200	°C
Total Device Power Dissipation (Derated above 25°C, see note 2)	Pdiss	14	W

Note: 1. Continuous operation at maximum junction temperature will affect MTTF
2.Bias Conditions should also satisfy the following expression: Pdiss < (Tj – Tc) / RJC and Tc = Tcase

Table 2. MSL Rating

Parameter	Rating	Standard
MSL – Moisture Sensitivity Level	Level 3	JEDEC Standard J-STD-020

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, RF CW operation	$R_{\theta JC}$	11	℃/W

Table 4. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=1.5mA	V_{DSS}		125		V
Gate Threshold Voltage	V_{DS} = 28V, I_D =1.5 mA	V_{GS}(th)		-2.7		V
Gate Quiescent Voltage	V_{DS} =28V, I_{DS}=50mA, Measured in Functional Test	$V_{GS(Q)}$		-2.24		V

Functional Tests (In Test Fixture, 50 ohm system) : V_{DD} = 28 Vdc, I_{DQ} = 30 mA, f = 3.5GHz, Pulsed CW, 20uS/10%

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain@P1dB	Gp		18.4		dB
Drain Efficiency @ P_{SAT}	Eff		66.6		%
Saturated Power	P_{SAT}	38	39.5		dBm
Input Return Loss	IRL		-8		dB
Mismatch stress at all phases (Device no damage)	VSWR		10:1		Φ

TYPICAL CHARACTERISTICS

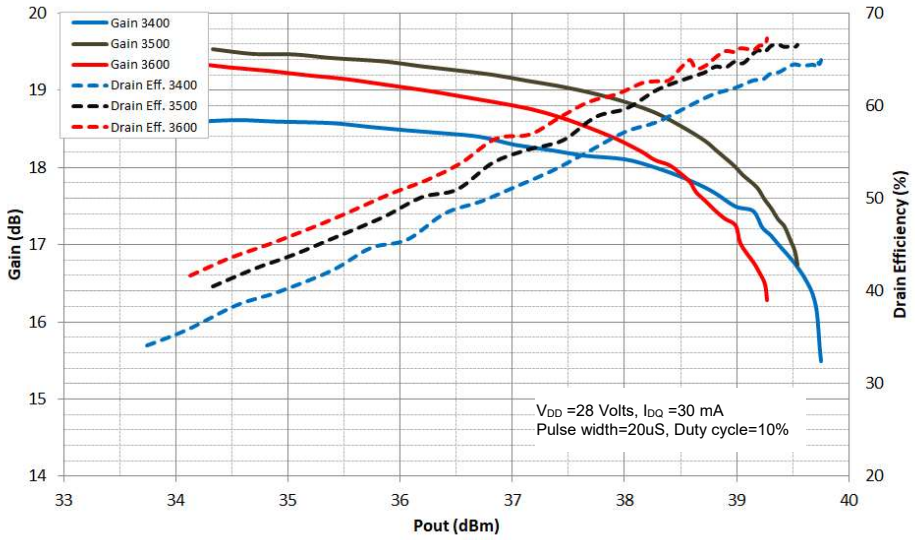


Figure 1. Power Gain and Drain Efficiency as Function of Pulse Output Power (3400-3600MHz)

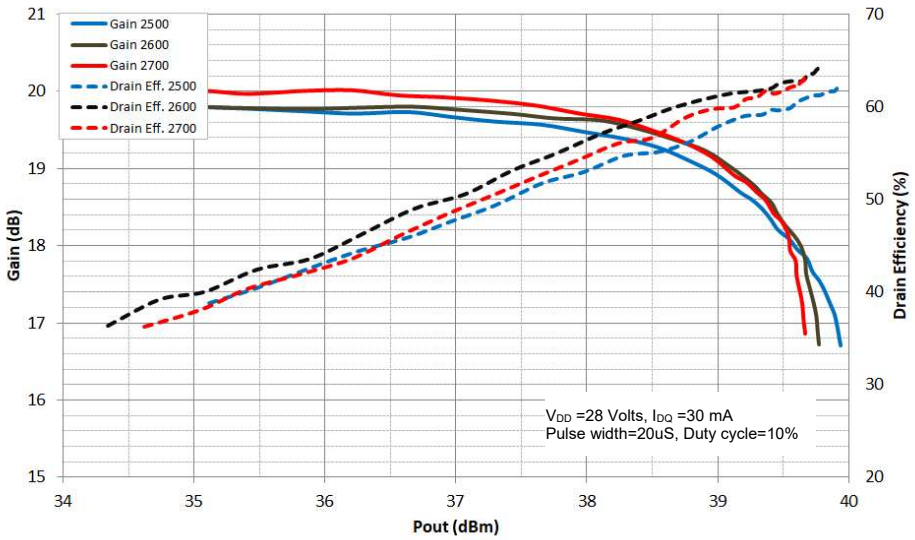


Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power (2500-2700MHz)

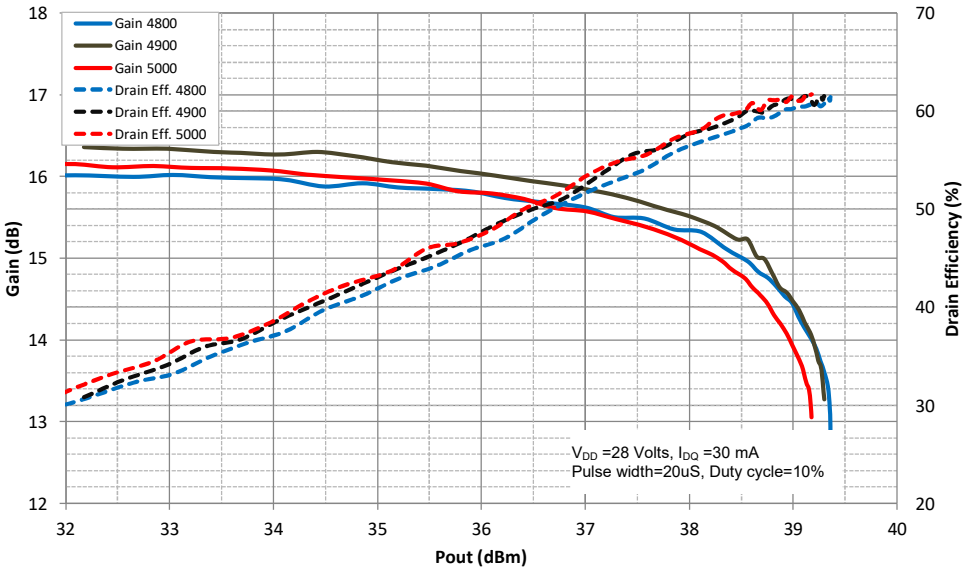


Figure 3. Power Gain and Drain Efficiency as Function of Pulse Output Power (4800-5000MHz)

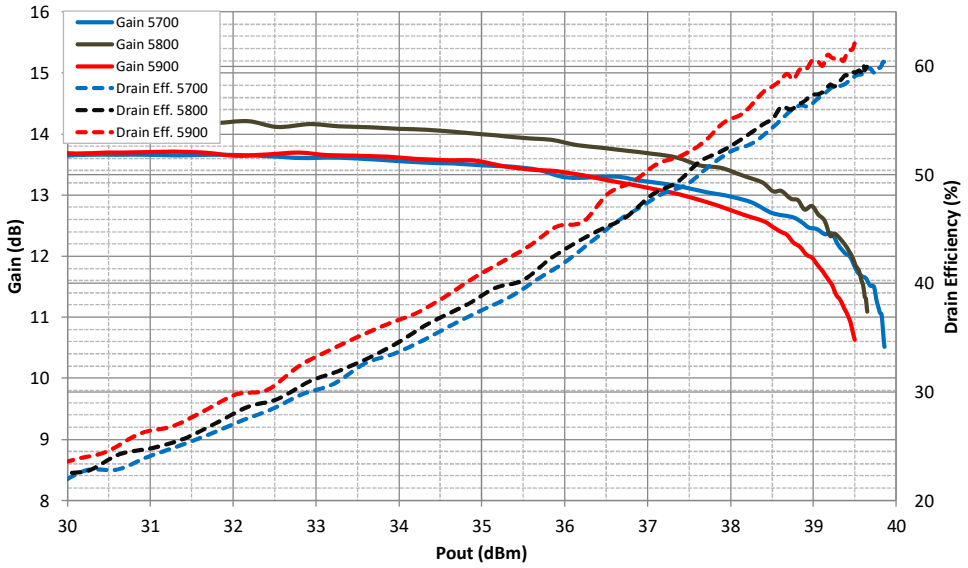


Figure 4. Power Gain and Drain Efficiency as Function of Pulse Output Power (5700-5900MHz)

Reference circuit of test fixture assembly diagram

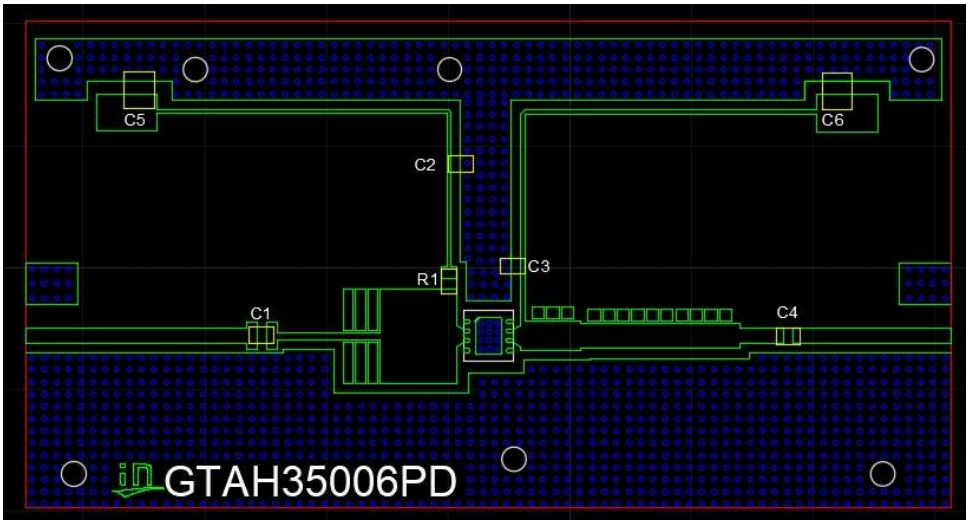


Figure 5. 3400-3600MHz fixture

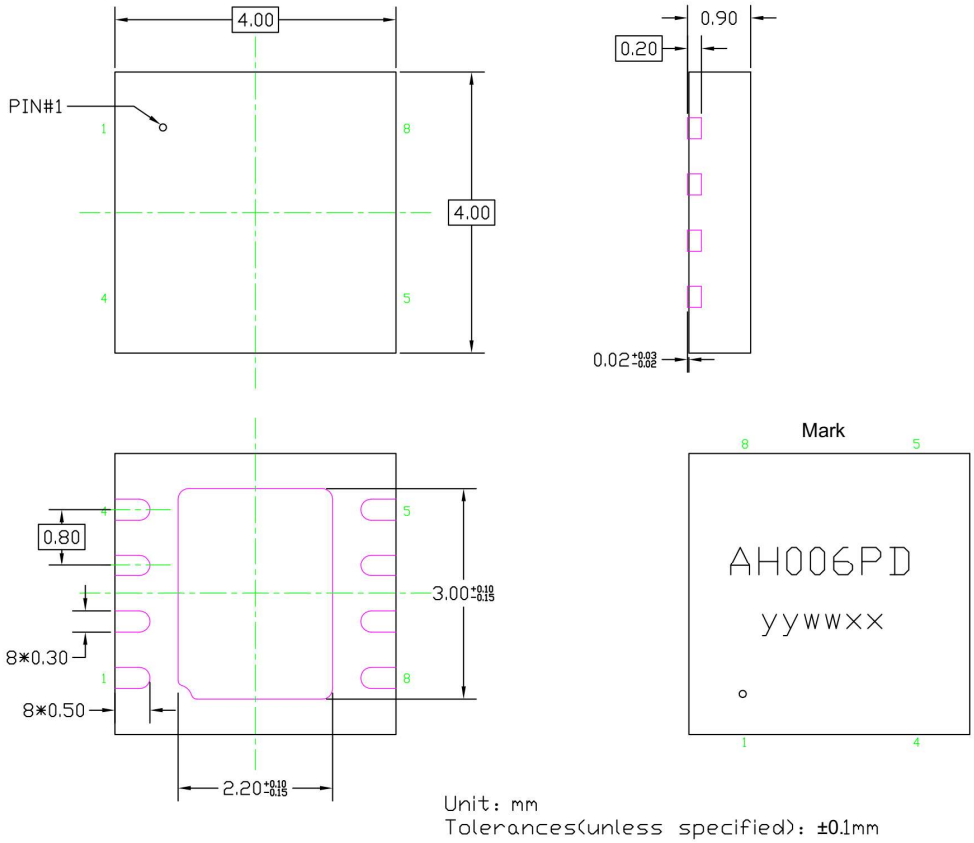
(note: other bands can reuse the same PCB layout)

Table 5: components designations and values of 3400-3600Mhz fixture

Component	Description	Suggested Manufacturer	P/N
C5、C6	10uF	TDK1206	
C1、C2、C4	8.2pF	ATC600S	
C3	6.8pF	ATC600S	
R1	10Ω	0603	
PCB	0.508mm [0.020"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper		

Package Dimensions

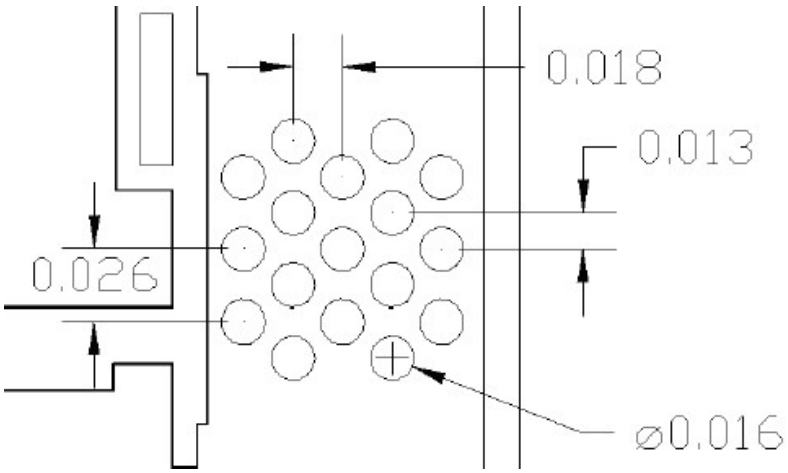
4*4 DFN Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.1mm.

Recommended vias layout: (all in inches)



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2019/9/11	V1.0	Preliminary Datasheet Creation
2019/11/6	V1.1	Add more data of other core bands
2024/4/20	V1.2	Add 2-4GHz application notice

Notice