MM2002A LDMOS TRANSISTOR

Document Number: MM2002A
Product Datasheet V1.0

20W, 3GHz General Purpose RF LDMOS FETs

MM2002A

Description

The MM2002A is a 20-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies up to 3 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

It can support CW, pulsed CW either saturated or linear operation.

- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 50 mA, CW.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2800	45.63	36.5	49.6	10.86	46.42	43.9	51.7
2850	45.02	31.8	51.5	11.65	45.83	38.3	53.6
2900	44.05	25.4	49.4	11.6	44.89	30.8	51.8

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- General purpose power amplifier
- L, S band power amplifier

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.6	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=500uA	$V_{(BR)DSS}$	65	70		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS(th)}$	——	1.98	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 50 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.53	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		23.5		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		9.7		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		0.7		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 50 mA, f = 2900 MHz

VSWR 10:1 at 20W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1. Network analyzer output S11/S21 (VDS=28V IDQ=250mA VGS=3.75V)

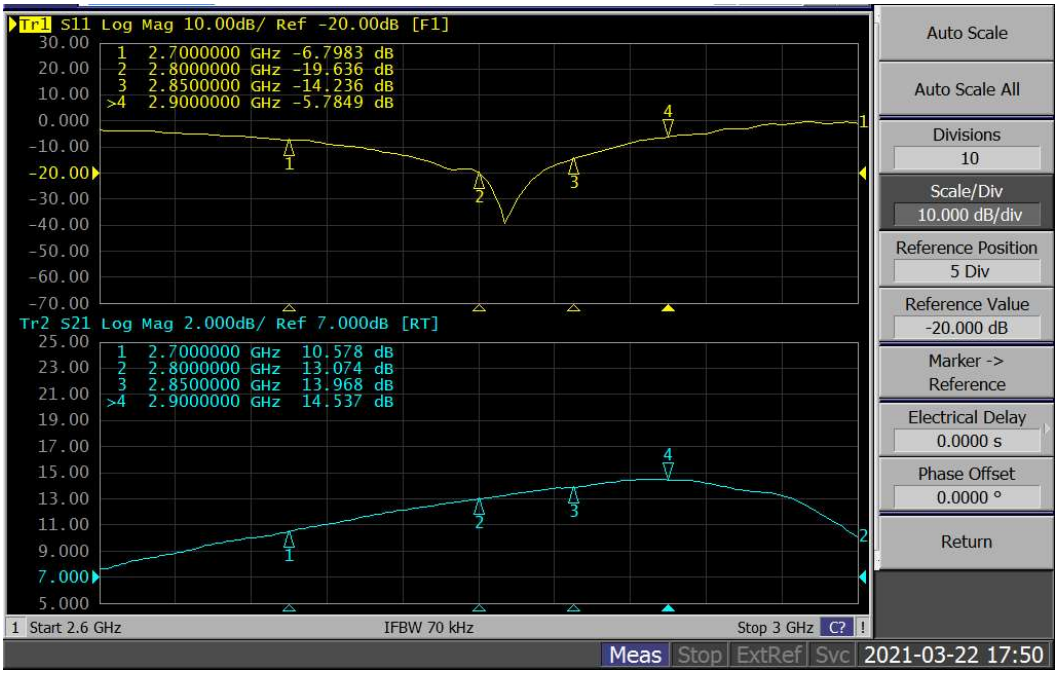


Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power

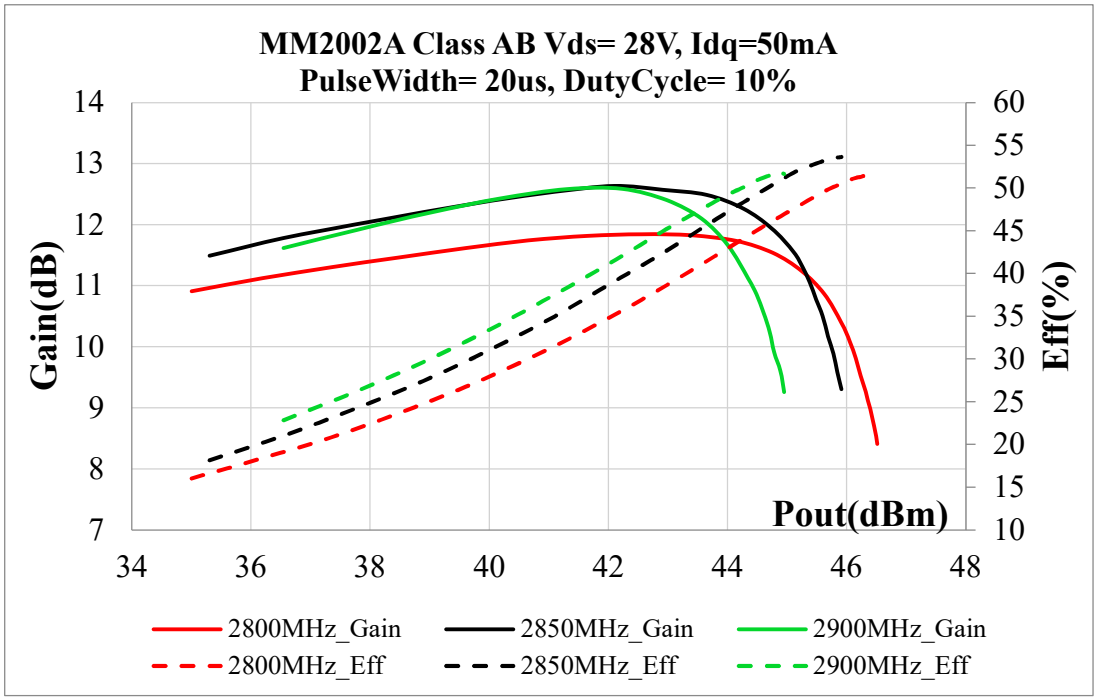


Figure 3. Test Circuit Component Layout (PCB: 20 Mils, RO4350B）

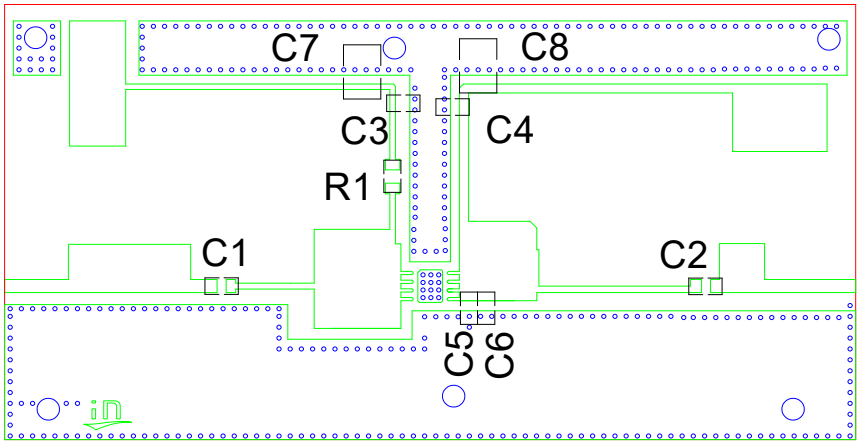
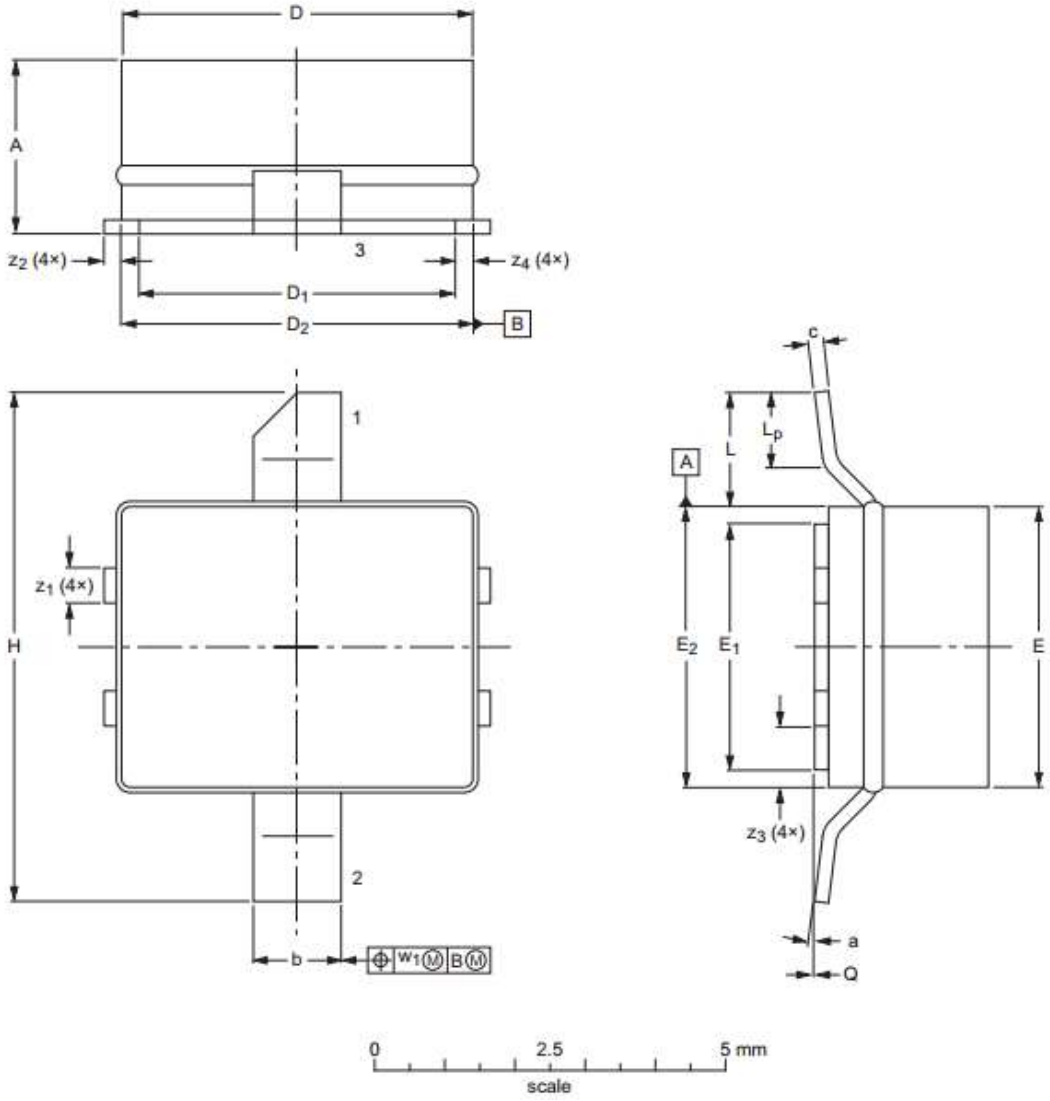


Table 4. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	3.9pF	0603	1
C2, C3, C4	8.2pF	0603	3
C5	0.5pF	0603	1
C6	0.3pF	0603	1
C7, C8	10uF/100V	1210	2
R1	10ohm	0603	1

Package Outline

Earless Flanged ceramic package; 2 leads(1-Drain,2-Gate,3-Source)



UNIT	A	b	c	D	D_1	E	E_1	E_2	H	L	L_P	Q	w_1	z_1	z_2	z_3	z_4	α
mm	2.34	1.35	0.23	5.16	4.65	4.14	3.63	4.14	7.49	2.03	1.02	0.1	0.25	0.58	0.25	0.97	0.51	7°
	2.13	1.19	0.18	5.00	4.50	3.99	3.48	3.99	7.24	1.27	0.51	0.0		0.43	0.18	0.81	0.00	0°

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-MM					18/6/2014

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/3/17	Rev 1.0	Product Datasheet

Application data based on LSM-21-07

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