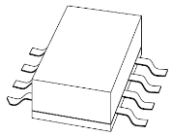
M8M1001 LDMOS TRANSISTOR

Document Number: M8M1001
Preliminary Datasheet V1.0

10W, 28V High Power RF LDMOS FETs

M8M1001



Description

The M8M1001 is a 10-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies up to 2 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

- Typical Performance (On Innogration fixture with device soldered):
  V_{DD} = 28 Volts, I_{DQ} = 100 mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	η_D@P_{-1} (%)
960 MHz	23	13	63

- Typical Performance (On Innogration fixture with device soldered):
  V_{DD} = 12 Volts, I_{DQ} = 10 mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	η_D@P_{-1} (%)
120 MHz	13	5	58

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class

Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		95		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}			1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 50 μA)	V_{GS}(th)		2.07		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.3		V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		TBD		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		TBD		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		TBD		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 100mA, f = 960 MHz, CW Signal Measurements.

Power Gain	Gp	———	23	———	dB
Drain Efficiency@P1dB	η_D	———	63	———	%
1 dB Compression Point	P_{-1dB}	———	13	———	W
Input Return Loss	IRL	———	-7	———	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 960 MHz

VSWR 20:1 at 13W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

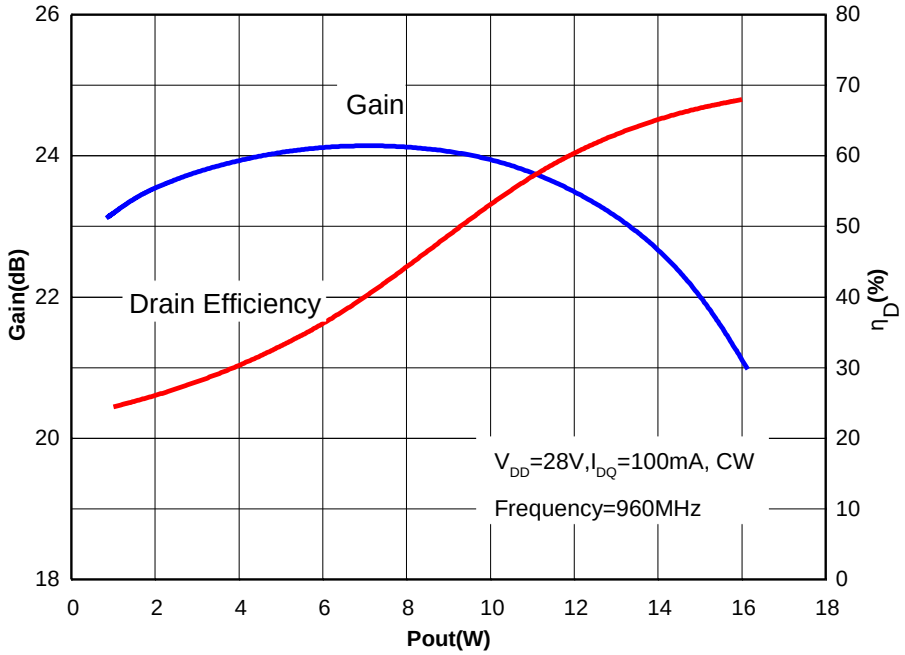


Figure 1. Power gain and drain efficiency as function of Power out

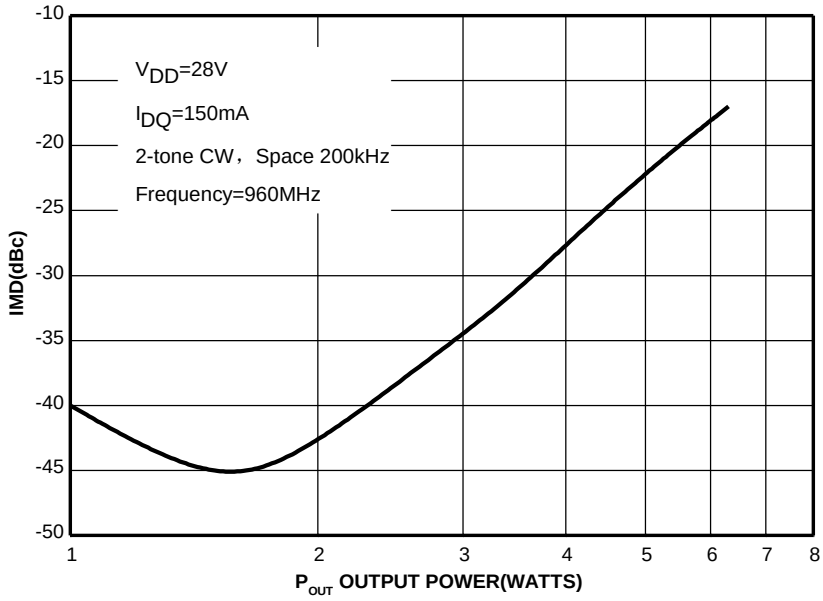
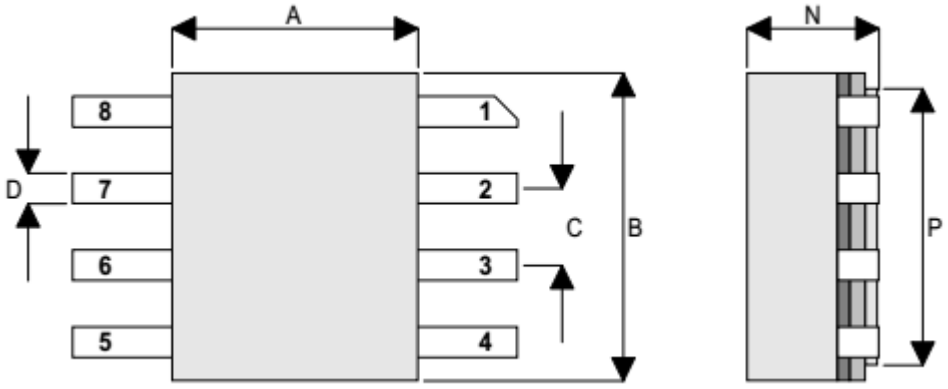
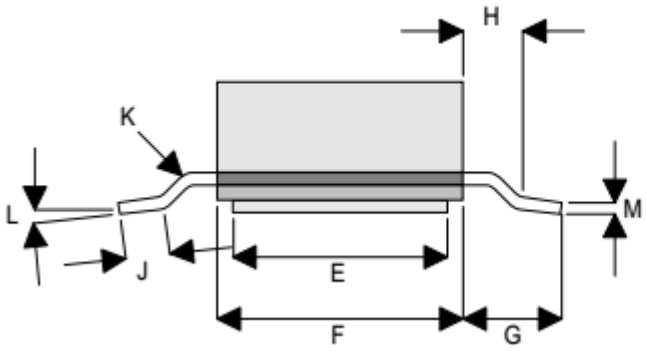


Figure 2. IMD3 versus Output Power

Package Outline

SO8 Ceramic package; Gull-wing 8 leads





Pin Connection

Pin1—Source	Pin5—Source
Pin2—Drain	Pin6—Gate
Pin3—Drain	Pin7—Gate
Pin4—Source	Pin8—Source
Bottom—Source	

UNIT	A	B	C	D	E	F	G	H	J	K	L	M	N	P
mm	4.06	5.08	1.27	0.51	3.56	4.06	1.65	0.76	0.51 1.02	45°	0° 7°	0.20	2.18	4.57
Tol.	±0.08	±0.08	±0.08	±0.08	±0.08	±0.08	±0.08	0.25 0	Min. Max.	Max.	Min. Max.	±0.08	±0.08	±0.08
Inches	0.160	0.200	0.050	0.020	0.140	0.160	0.065	0.030	0.020 0.040	45°	0° 7°	0.008	0.086	0.180
Tol.	±0.003	±0.003	±0.003	±0.003	±0.003	±0.003	±0.003	0.010 0	Min. Max.	Max.	Min. Max.	±0.003	±0.003	±0.003

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-M8G					5/6/2017

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/12/17	Rev 1.0	Preliminary Datasheet

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