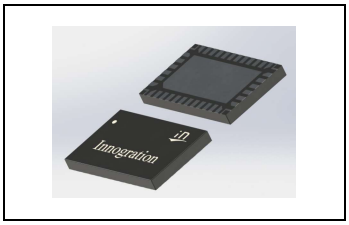
3.4-3.8GHz, 50W, 31V GaN PA Module

Description



The GMAH3438-50 is a 50-watt peak power, integrated 2-stage Power Amplifier Module, designed for massive MIMO applications, with frequencies from 3.4 to 3.8GHz.

The module is 50 Ω input fully matched and output partially matched, and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions. The module incorporates an asymmetrical Doherty final stage and its driver, delivering high power added efficiency for the entire module at 8W average power. Compared to the closest LDMOS MMIC solution, it can support much wider bandwidth up to 400MHz and maintain at least 10% higher efficiency relatively.

Innogration owns the patents for internal Doherty architecture, and related plastic open cavity.

- Typical Performance of Doherty Demo (On Innogration fixture):

$V_{D1、2}$ =31 V, I_{DQ1} =30 mA, I_{DQ3} =50 mA, V_{G2}=-4.2V .

Freq(MHz)	Pout(dBm)	CCDF(dB	Ppeak(dBm)	Ppeak(W)	ACPR(dBc)	Gain(dB)	Efficiency(%)
3400	39.01	8.42	47.42	55.27	-30.42	29.68	48.91
3600	38.98	8.70	47.68	58.58	-28.46	30.48	50.49
3800	38.99	8.52	47.50	56.28	-29.68	29.15	48.91

Notes:

(1) WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz,PAR =10.5 dB at 0.01 % probability on CCDF.

(2) Data within narrower band like 3.4-3.6/3.5-3.7/3.6-3.8G indicated 2% higher back off efficiency

Features

- N77/N78 power amplifier
- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- 50 Ω Input fully matched
- Integrated Doherty Final Stage
- 6x10 mm Surface Mount Open plastic Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Pin Configuration and Description

Pin No.	Symbol	Description
6	RF IN	RF Input
1	VDS-driver	Driver stage, Drain Bias
4	VGS-driver	Driver stage, Gate Bias
19,21	RF Out2	RF Output，Main Amplifier
22,24	RF Out1	RF Output, Peaking Amplifier
11	VGS-main	Main Amplifier, Gate Bias
16,17	VDS-main	Main Amplifier, Drain Bias
32	VGS-peak	Peaking Amplifier, Gate Bias
26,27	VDS-Peak	Peaking Amplifier, Drain Bias
3,8-10,14,15,28,29,33-35	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36	GND	Internal Grounding, recommend connecting to Epad ground
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	150	Vdc
Gate--Source Voltage	V_{GS}	-10 to +1	Vdc
Operating Voltage	V_{DD}	+40	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance@Average Power, Junction to Case Tcase=+85℃，CW Test，Pdiss=9W，Pout=8W,	$R_{\theta JC}$	TBD	°C/W

Notes:
(1) The thermal resistance is acquired by our company's FEA model,which was calibrated by IR measurement,the value shall be applied to reliability.
(2) The reference Tcase temperature 85℃ is apply on the backside of package.
(3) The device soldering onto the 20mil Rogers PCB with 50×Φ0.4mm via hole beneath the package backside and the reference temperature Tcase（85℃） apply on the groundside of the PCB.
(4) The power dissipation in the table is overall dissipation which include Carrier PA, Peaking PA and driver PA.

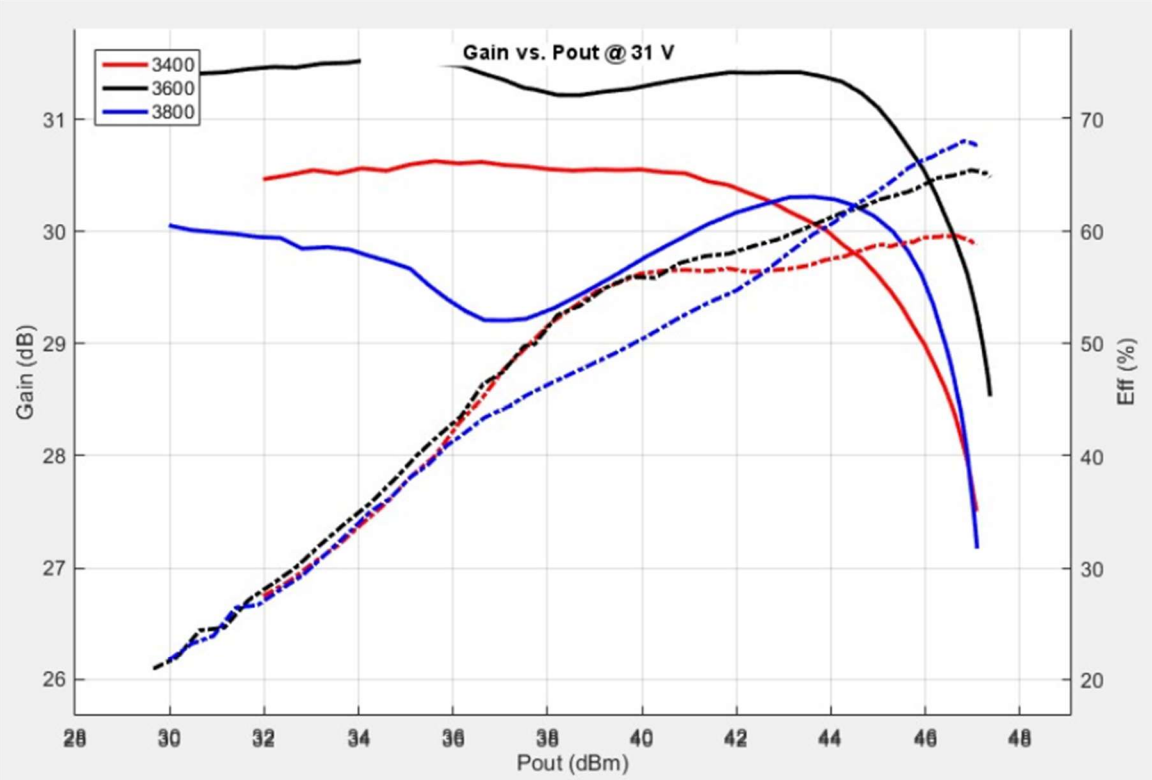
Table 3. ESD Protection Characteristics

Test Methodology	Class Voltage
Human Body Model(HBM) (JEDEC Standard JESD-A114)	±225V
Charged Device Model (CDM) (JEDEC Standard JESD22-C101F)	±1000V

Load Mismatch of per Section (On Test Fixture, 50 ohm system): $V_{D1、2}$=28 V, I_{DQ1} =30mA, I_{DQ3} =50mA, V_{G2}=-4.2V, f = 3.7 GHz

VSWR 10:1 at P3dB pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

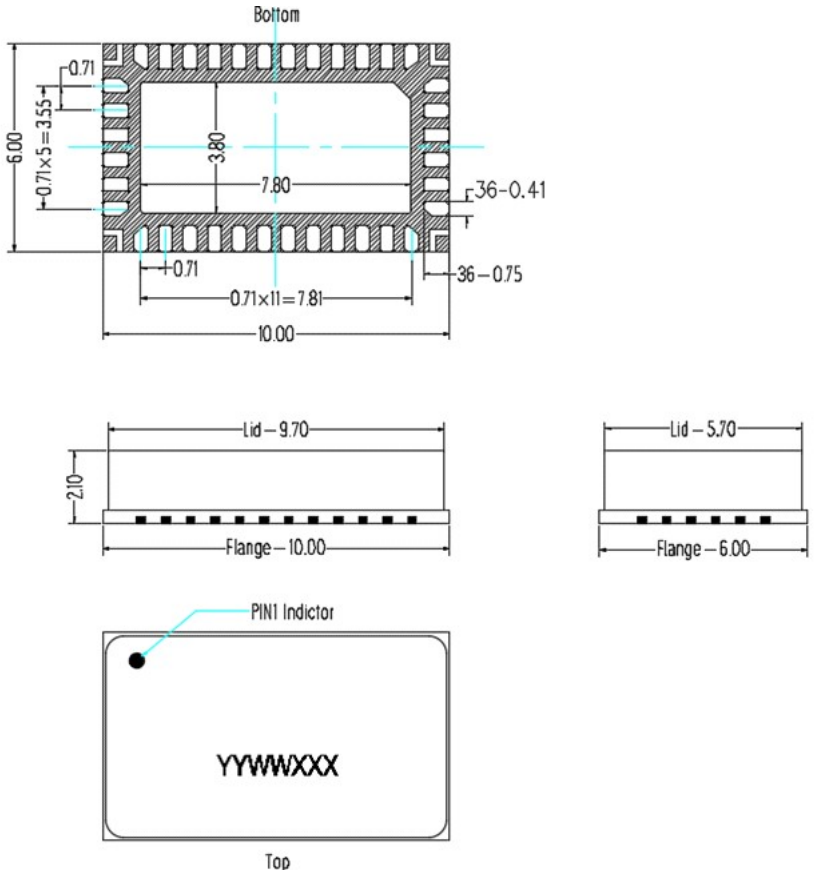


Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
3400	45.00	31.63	58.74	29.60	47.08	51.07	58.81
3600	46.23	41.95	64.68	30.33	47.37	54.57	64.79
3800	46.38	43.40	67.16	29.06	47.09	51.22	67.70

Figure 1. Power Gain and Drain Efficiency as Function of Pulse Output Power

Package Dimensions

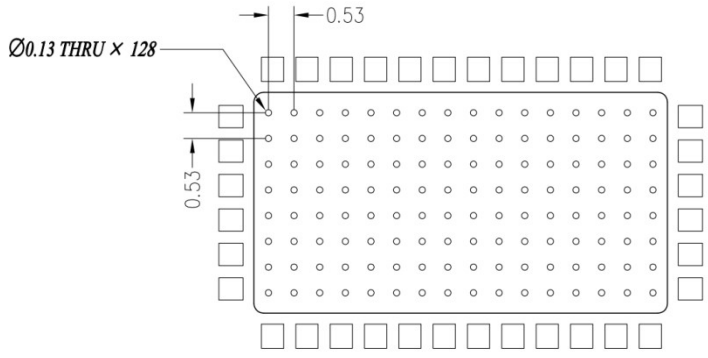
10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2021/2/26	Rev 1.0	Preliminary Datasheet

Application data based on LWH-21-03

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