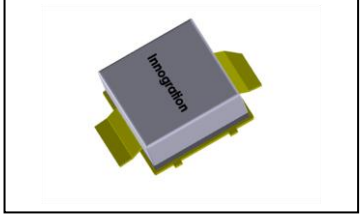
700MHz-2700MHz, 30W, 28V RF Power LDMOS FETs

Description

The ITCH27025E2 is a 30-watt, internally matched LDMOS FET, designed for cellular base station and ISM applications with frequencies from 700MHz to 2700 MHz

ITCH27025E2



- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 250 mA , Pulse Width =10us, Duty Cycle =12%.

	Frequency (MHz)	Gp @ P_1dB (dB)	P_1dB (dBm)	η_D (%)	P_3dB (dBm)	η_D (%)
2.6G Demo	2500	17.5	45.5	49.7	46.5	52.5
	2600	18.3	45.0	52.5	46.0	55.9
	2700	19.2	43.8	51.8	44.8	53.7
1.5G Demo	1470	19.2	45.9	61.4	46.4	63.4
	1500	19.3	45.4	63.7	46.2	66.4
	1530	18.7	44.7	61.3	45.5	63.1

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-7 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	TBD	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit

Drain-Source Breakdown Voltage	V_{GS}=0 V; I_{DS}=500 μA	V_{DSS}	65			V
Zero Gate Voltage Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}			1	μA
Gate--Source Leakage Current	V_{GS} = 9 V, V_{DS} = 0 V	I_{GSS}			1	μA
Gate Threshold Voltage	V_{DS} = 28V, I_D = 600 μA	$V_{GS(th)}$		2.05		V
Gate Quiescent Voltage	V_{DS} = 28 V, I_{DS} = 250 mA, Measured in Functional Test	$V_{GS(Q)}$		2.8		V

Pulse CW Signal performance (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 250 mA, f = 1500 MHz, Pulse CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P1dB	Gp		19.3		dB
Drain Efficiency@P3dB	η_D		66.4		%
3dB Compression Point	P_{-3dB}		46.2		dBm
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 250 mA, f = 1500 MHz

VSWR 10:1 at 30W Pulsed CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

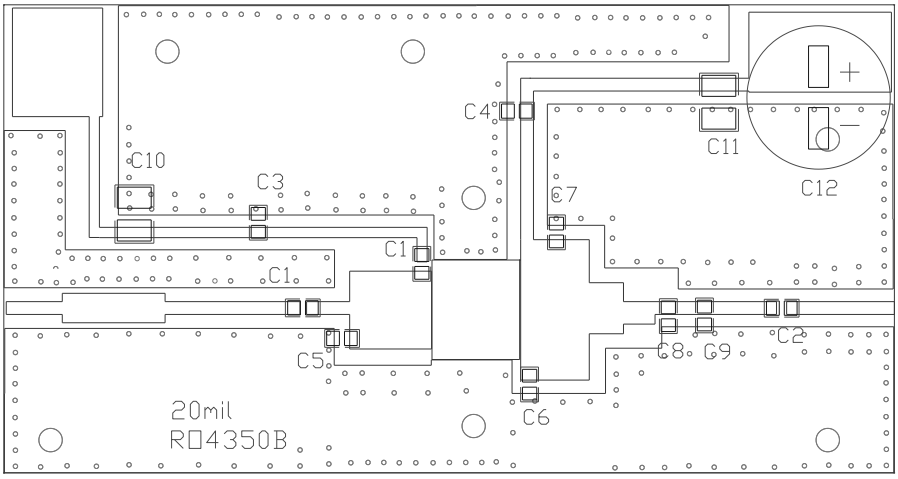


Figure 1. Test Circuit Component Layout(2500~2700MHz)

Table 5. Test Circuit (2500~2700MHz) Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	3.9pF	0603	1
C2, C3, C4	12 pF	0603	3
C5, C8, C9	1.0pF	0603	3
C6	1.5pF	0603	1
C7	1.8pF	0603	1
C10, C11	10uF/100V	1210	2
C13	100uF/63V		1
R1	10ohm	0603	1
PCB	0.508mm [0.020"] thick, εr=3.48, Rogers RO4350, 1 oz. copper		

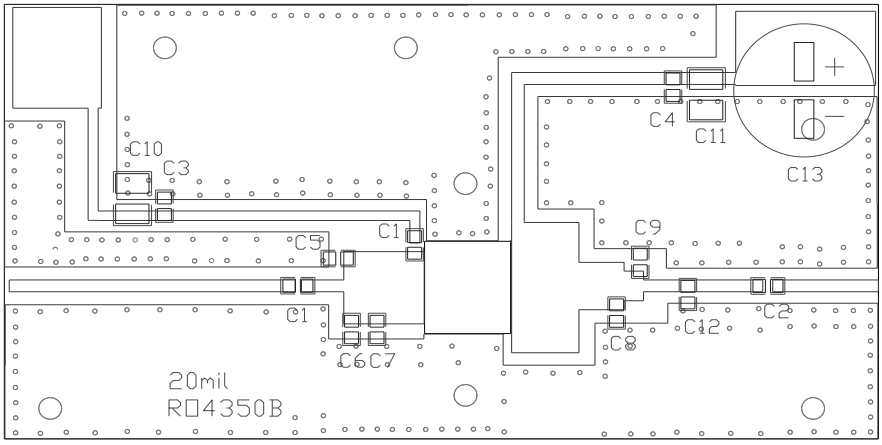


Figure 2. Test Circuit Component Layout(1475~1530MHz)

Table 6. Test Circuit (1475~1530MHz) Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	3.9pF	0603	1
C2, C3, C4	27 pF	0603	3
C5, C8, C9	2.0pF	0603	3
C6, C12	3.9pF	0603	2
C7	1.0pF	0603	1
C10, C11	10uF/100V	1210	2
C13	100uF/63V		1
R1	10ohm	0603	1
PCB	0.508mm [0.020"] thick, εr=3.48, Rogers RO4350, 1 oz. copper		

TYPICAL CHARACTERISTICS

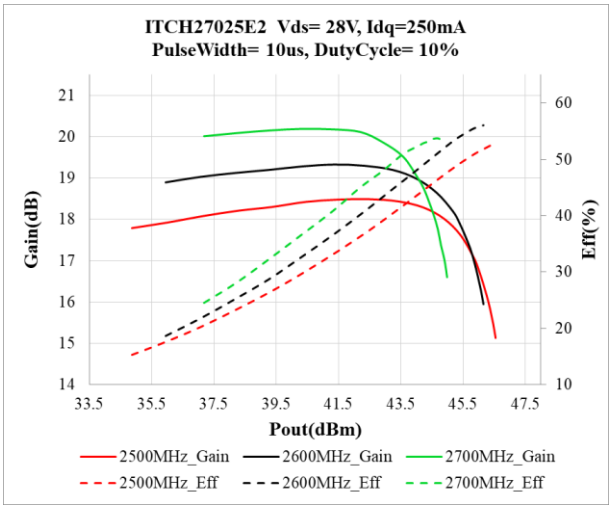


Figure 3. Power gain and drain efficiency as function of Pulse output power（2500-2700MHz）

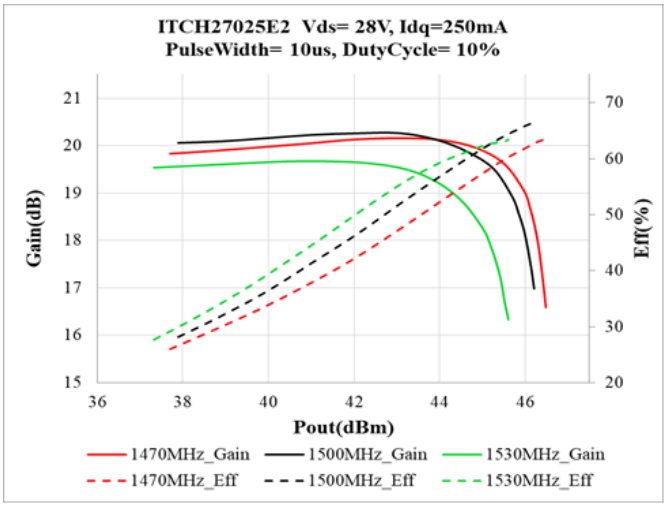
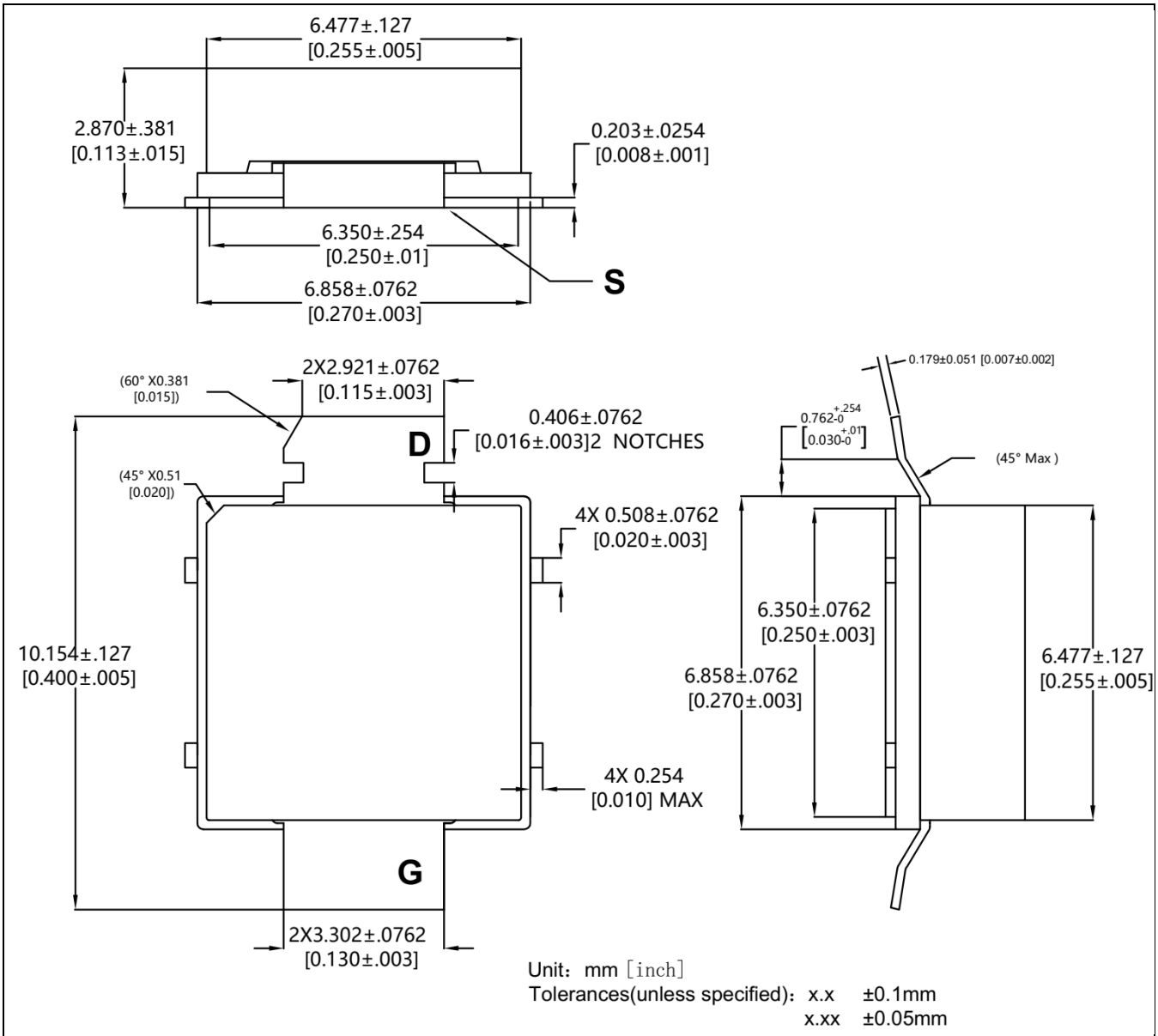


Figure 4. Power gain and drain efficiency as function of Pulse output power（1470-1530MHz）

Package Outline



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-E2					2020-4-21

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2021/03/01	Rev 1.0	Preliminary Datasheet

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