

SME6005V GaN TRANSISTOR

Document Number: SME6005V
Preliminary Datasheet V1.0

Gallium Nitride 50V 50W, RF Power Transistor

Description

The SME6005V is a 50-watt, unmatched GaN HEMT, designed for multiple applications with frequencies up to 4000MHz.

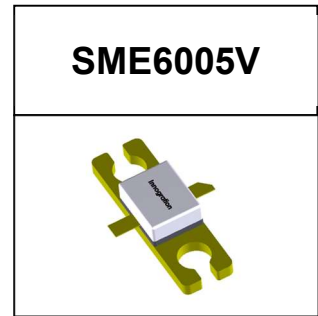
It can support CW, pulsed and any modulation applications

There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

- Typical performance (on fixture with device soldered):

$V_{DS}=50V$ $I_{DQ}=10mA$, Pulse CW, Pulse Width=100us, Duty cycle=10% ..

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	Eff(%)
3400	35.55	48.25	66.8	0.2	12.7	66.83%
3450	35.05	47.91	61.8	0.19	12.86	65.05%
3500	35.54	47.65	58.2	0.18	12.11	64.68%
3550	35.88	47.5	56.2	0.17	11.62	66.16%
3600	35.6	47.32	54.0	0.16	11.72	67.44%



Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to 0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum forward gate current	Igf	7.5	mA
Storage Temperature Range	Tstg	-65 to +150	C
Case Operating Temperature	T_C	-55 to +150	C
Operating Junction Temperature	T_J	+225	C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C=85^{\circ}C$, $T_J=200^{\circ}C$, DC Power Dissipation, FEA	$R_{\theta JC}$	5	$^{\circ}C/W$

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Preliminary Datasheet V1.0

Table 3. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8\text{V}; I_{DS}=7.5\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}, I_D = 7.5\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}, I_{DS}=10\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

Functional Tests (In Innogration broadband Test Fixture, 50 ohm system) : $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 10\text{mA}$, $f = 3500\text{MHz}$, CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P3dB	Gp		11.5		dB
Drain Efficiency@P3dB _t	Eff		63		%
3dB Compressed point	P3dB		47		dBm
Input Return Loss	IRL		-7		dB
Mismatch stress at all phases(No device damage)	VSWR		10:1		ϕ

Reference Circuit of Test Fixture Assembly Diagram

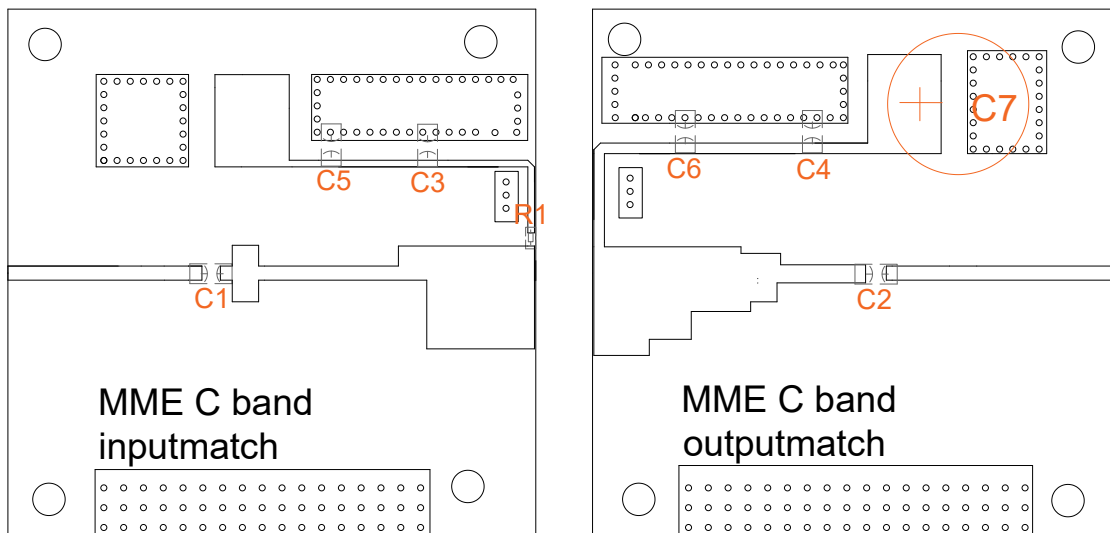


Figure 1. Test Circuit Component Layout (3400MHz~3600MHz)

Table 4. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1,C2,C3,C4	6.8pF	0805
C5 C6	Ceramic multilayer capacitor, 10uF, 100V	DLC75D
C7	470uF,63V	
R1	Chip Resistor,9.1 Ω	0603
PCB	0.508mm [0.020"] thick, $\epsilon_r=3.48$, Rogers RO4350B, 1 oz. copper	

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Figure 3. Network Analyzer result S11 and S21 (3400MHz~3600MHz)

Vds=50V Idq=100mA Vgs=-3V Input Power = 0dBm



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Package Outline

Flanged ceramic package; 2 leads

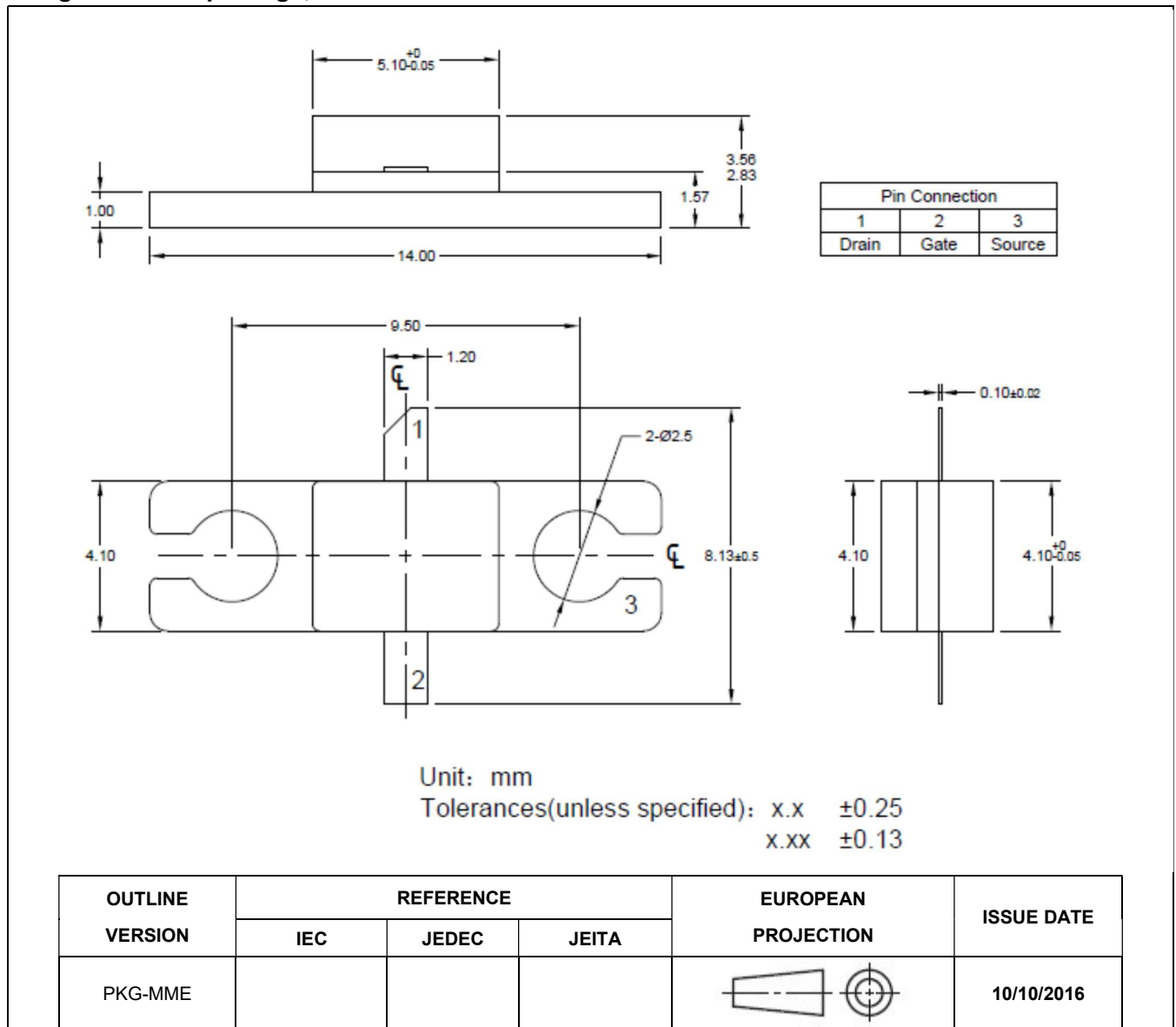


Figure 1. Package Outline PKG-MME

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Preliminary Datasheet V1.0

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/2/4	V1.0	Preliminary Datasheet Creation

Application data based on HL-21-17

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