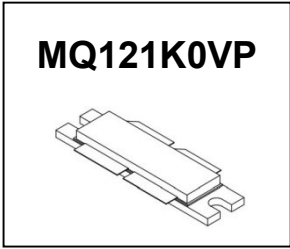


# MQ121K0VP LDMOS TRANSISTOR

Document Number: MQ121K0VP  
Preliminary Datasheet V1.0

## 1000W, 50V Avionics RF LDMOS FETs



### Description

The MQ121K0VP is a 1000W, high performance, internally matched LDMOS FET, designed for avionics applications with frequencies 960-1215MHz. It is featured for high power and high ruggedness.

**It is recommended to use this device under pulse condition only**

- Typical Pulse Performance (on innogration wide band test fixture with device soldered):  
Vds = 50 V, Idq = 100 mA, TA = 25 °C, Pulse condition: 1%, 10us

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
960	60.66	1164.0	49.5	12.95	61.39	1377.1	51.3
1030	59.85	965.8	49.9	13.87	60.72	1180.8	51.6
1090	59.9	976.3	51.9	14.08	60.62	1154.0	52.6
1130	59.76	945.4	49.4	13.45	60.49	1119.9	50.0
1160	59.76	946.8	48.5	11.53	60.48	1116.5	49.2
1180	59.96	990.8	49.5	12.57	60.55	1135.6	50.1
1200	60.19	1043.9	50.3	12.24	60.77	1194.2	50.2
1215	59.87	970.9	49.7	12.16	60.57	1139.8	50.1

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCl drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	115	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-10 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+55	Vdc
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>c</sub>	+150	°C
Operating Junction Temperature	T <sub>j</sub>	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case, Case Temperature 80°C, 870W Pout, Pulse width: 100us, duty cycle: 10%, Vds=50 V, Idq = 100 mA	R <sub>θJC</sub>	0.02	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

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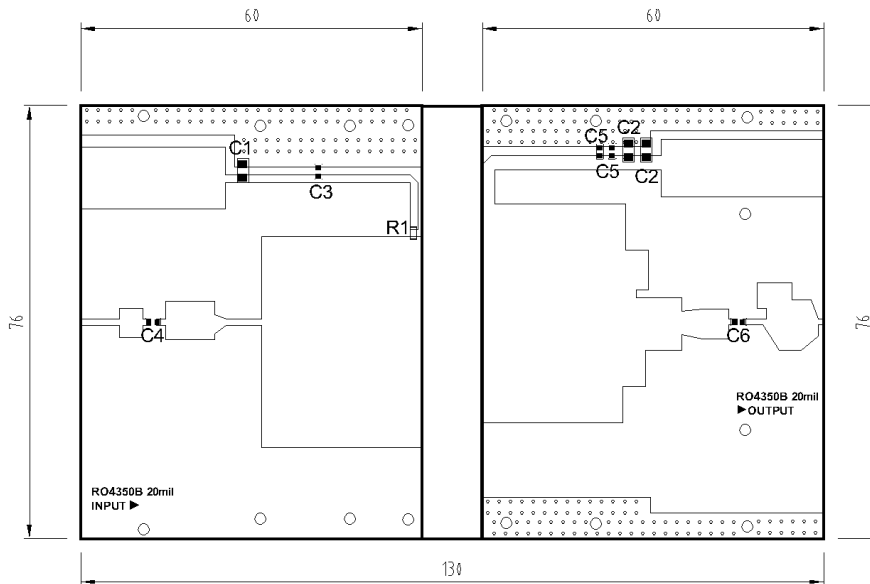
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**Table 4. Electrical Characteristics** (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>DC Characteristics</b>					
Drain-Source Breakdown Voltage (V <sub>GS</sub> =0V; I <sub>D</sub> =100uA)	V <sub>DSS</sub>	115			V
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V)	I <sub>DSS</sub>			10	μA
Gate--Source Leakage Current (V <sub>GS</sub> = 6 V, V <sub>DS</sub> = 0 V)	I <sub>GSS</sub>			1	μA
Gate Threshold Voltage (V <sub>DS</sub> = 50V, I <sub>D</sub> = 600 uA)	V <sub>GS(th)</sub>		1.6		V
Gate Quiescent Voltage (V <sub>DD</sub> = 50 V, I <sub>DQ</sub> = 100 mA, Measured in Functional Test)	V <sub>GS(Q)</sub>		3		V

## Reference Circuit of Test Fixture

(Layout file upon request) PCB: Roger 4350B, 20mils



**Figure 1. Test Circuit Component Layout**

Component	Description	Suggested Manufacturer
C1,C2	Ceramic multilayer capacitor, 10uF, 100V	10uF/100V
C3,C5	47pF	ATC800B
C4	100pF	ATC800B
C6	51pF	ATC800R
R1	Chip Resistor,9.1Ω,1206	
PCB	20mil thickness, εr=3.5, Ro4350B, 1 oz. copper	

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## TYPICAL CHARACTERISTICS

Figure 2: Power gain and Efficiency as a Function of Pout Pulse width:10uS, duty cycle: 1%, Vds = 50 V, Idq = 100 mA,

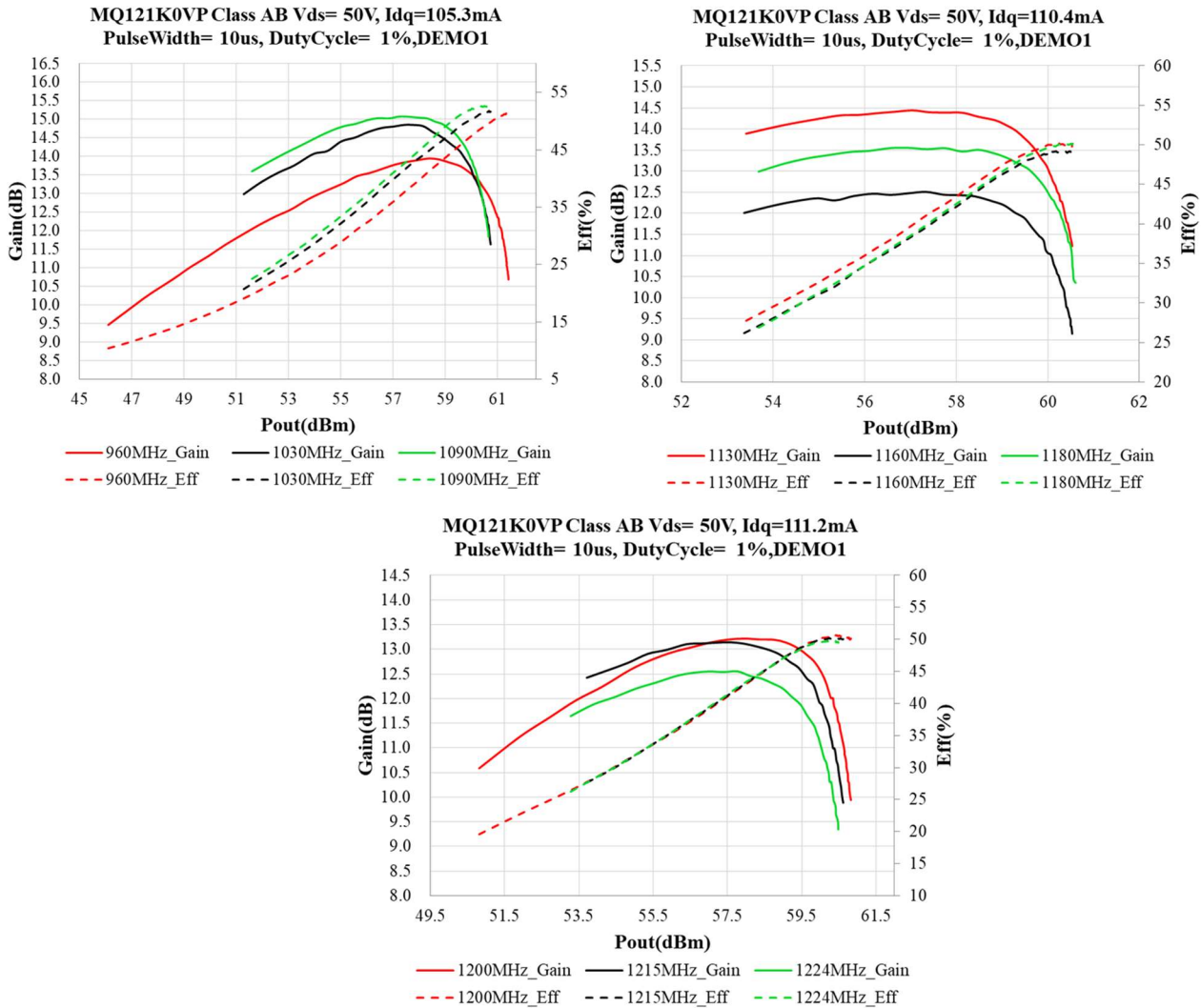
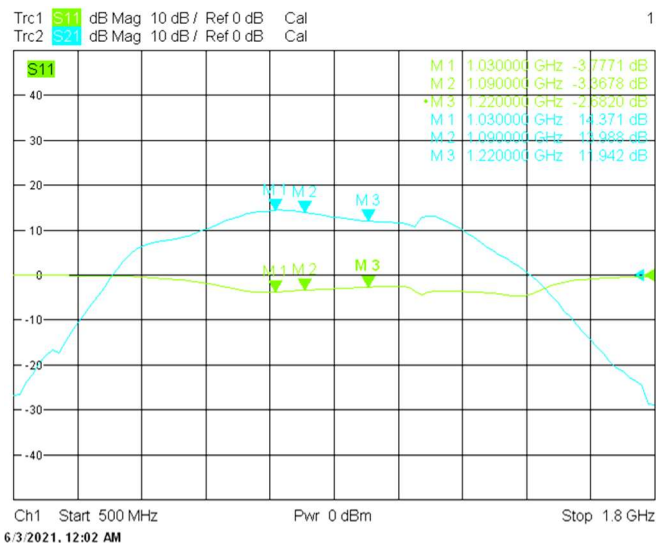


Figure 3: Network analyzer S11 and S21

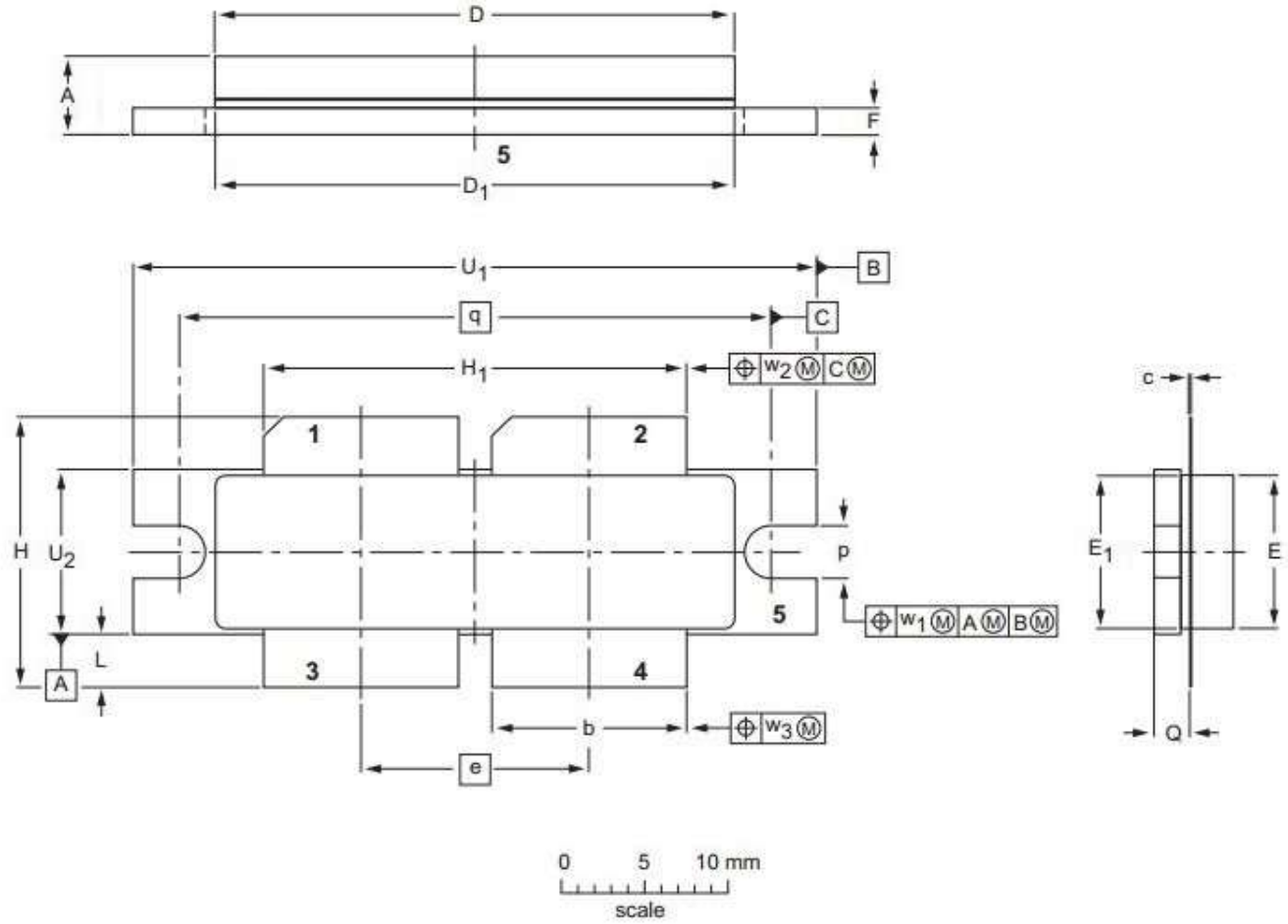


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## Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	W <sub>1</sub>	W <sub>2</sub>	W <sub>3</sub>
Mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
Inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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## Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2021/6/3	Rev 1.0	Preliminary Datasheet Creation

Application data based on JF-21-04

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