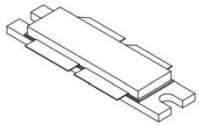
MQ121K0VP LDMOS TRANSISTOR

Document Number: MQ121K0VP
Preliminary Datasheet V1.0

1000W, 50V Avionics RF LDMOS FETs

MQ121K0VP



Description

The MQ121K0VP is a 1000W, high performance, internally matched LDMOS FET, designed for avionics applications with frequencies 960-1215MHz

It is featured for high power and high ruggedness.

It is recommended to use this device under pulse condition only

- Typical Pulse Performance (on innogration wide band test fixture with device soldered):
  Vds = 50 V, Idq = 100 mA, TA = 25 °C, Pulse condition: 1%, 10us

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
960	60.66	1164.0	49.5	12.95	61.39	1377.1	51.3
1030	59.85	965.8	49.9	13.87	60.72	1180.8	51.6
1090	59.9	976.3	51.9	14.08	60.62	1154.0	52.6
1130	59.76	945.4	49.4	13.45	60.49	1119.9	50.0
1160	59.76	946.8	48.5	11.53	60.48	1116.5	49.2
1180	59.96	990.8	49.5	12.57	60.55	1135.6	50.1
1200	60.19	1043.9	50.3	12.24	60.77	1194.2	50.2
1215	59.87	970.9	49.7	12.16	60.57	1139.8	50.1

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 870W Pout, Pulse width: 100us, duty cycle: 10%, Vds=50 V, I_{DQ} = 100 mA	$R_{\theta JC}$	0.02	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3		V

Reference Circuit of Test Fixture

(Layout file upon request) PCB: Roger 4350B, 20mils

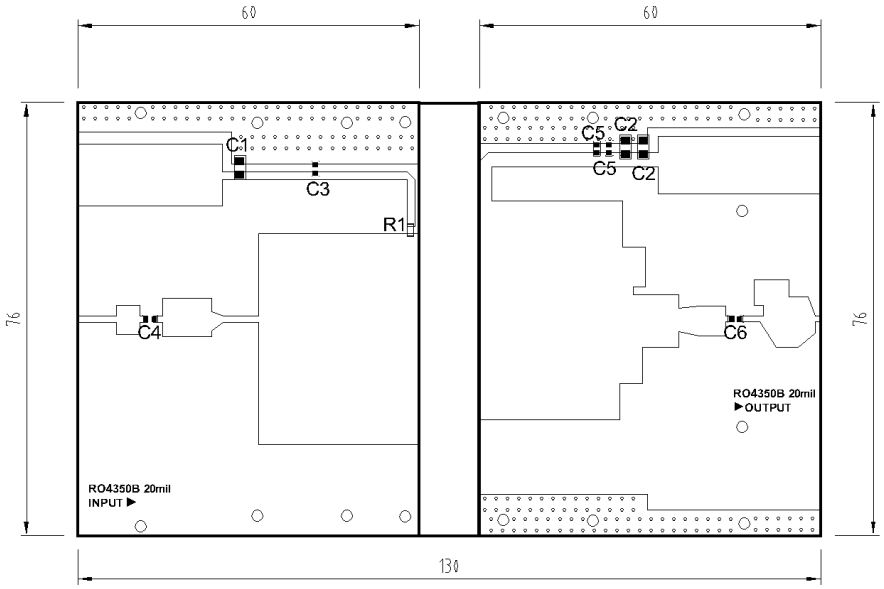
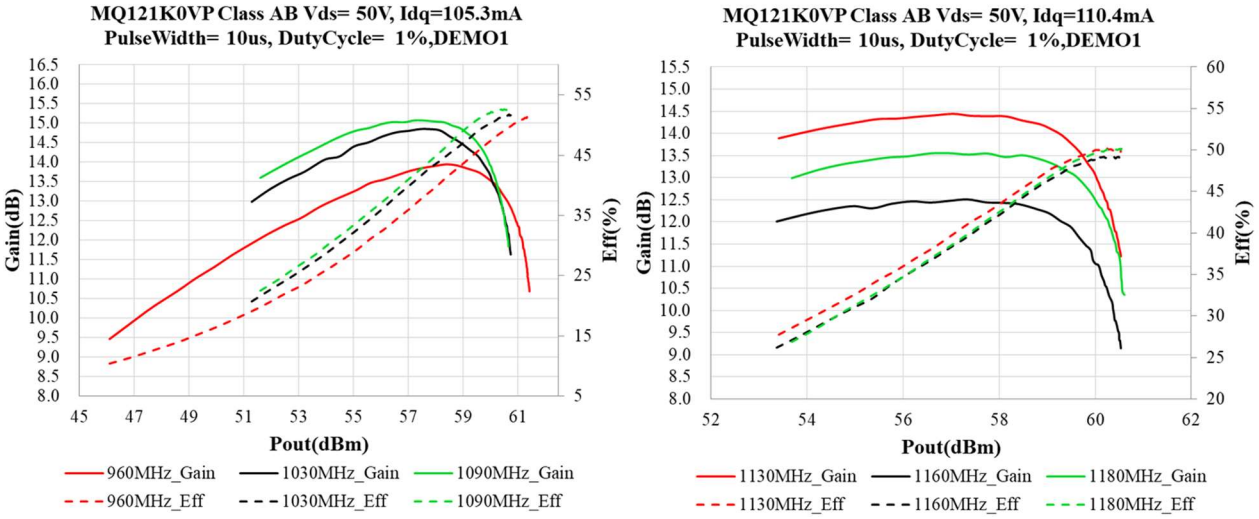


Figure 1. Test Circuit Component Layout

Component	Description	Suggested Manufacturer
C1,C2	Ceramic multilayer capacitor, 10uF, 100V	10uF/100V
C3,C5	47pF	ATC800B
C4	100pF	ATC800B
C6	51pF	ATC800R
R1	Chip Resistor,9.1Ω,1206	
PCB	20mil thickness, εr=3.5, Ro4350B, 1 oz. copper	

TYPICAL CHARACTERISTICS

Figure 2: Power gain and Efficiency as a Function of Pout Pulse width:10uS, duty cycle: 1%, Vds = 50 V, Idq = 100 mA,



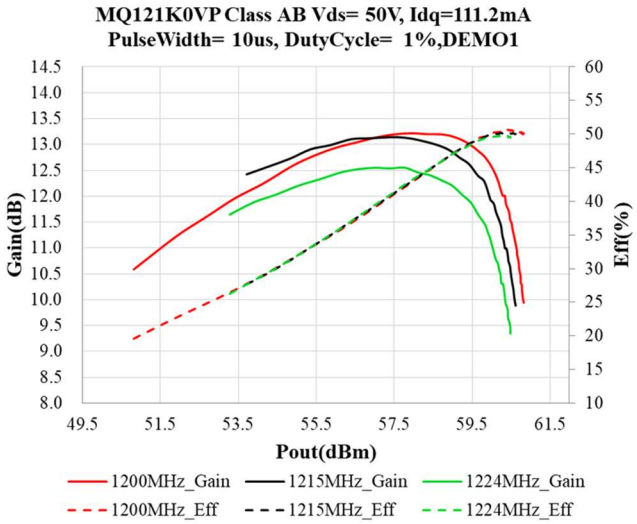
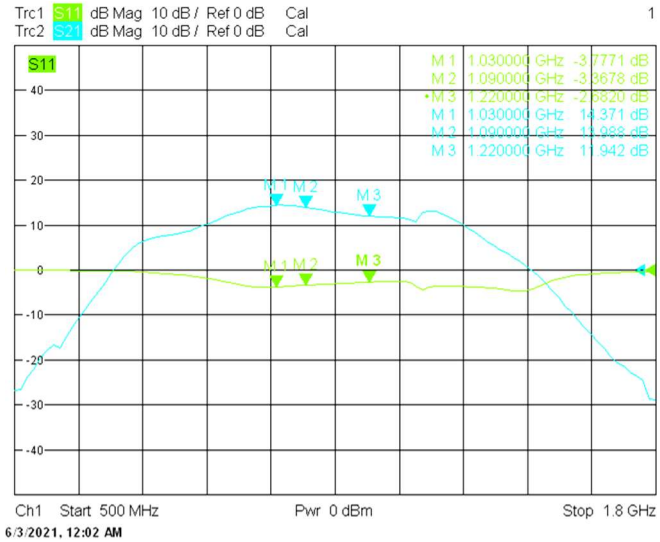
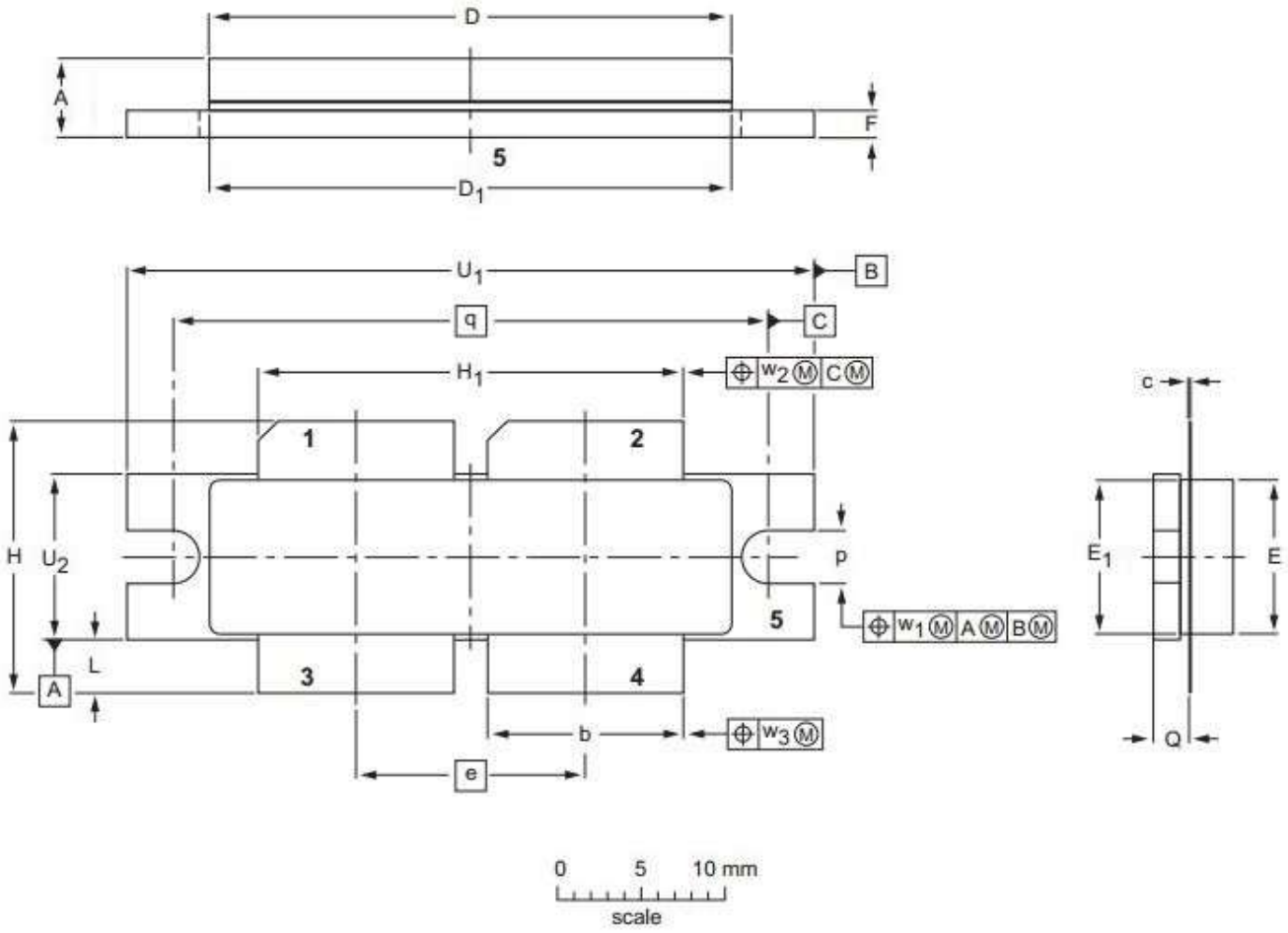


Figure 3: Network analyzer S11 and S21



Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
Mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
Inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2021/6/3	Rev 1.0	Preliminary Datasheet Creation

Application data based on JF-21-04

Disclaimers