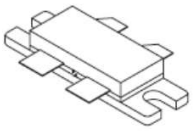
MK0530VPXS-F LDMOS TRANSISTOR

Preliminary Datasheet V1.0

300W, HF-0.5GHz 50V High Power RF LDMOS

MK0535VPXS-F



Description

The MK0535VPXS-F is a 300W Push Pull 50V LDMOS, unmatched for any applications within HF-0.5GHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

It can be the drop-in replacement of its equivalent 300W VDMOS like BLF278/MRF151G/VRF151G with higher efficiency, improved thermal performance and stability.

- Typical performance(on Innogration test board with device soldered)

  Signal: CW , Vgs=3.44v,Vds=50v,Idq=300mA

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	Ids(A)	Gain(dB)	Eff(%)
175	35.5	55.5	355	9.5	20	75

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	TBD	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics (per half section)

Drain-Source Voltage V_{GS}=0, I_{DS}=1.0Ma	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS}(th)$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 300 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.44	——	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)				mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}				pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}				pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}				pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 300 mA, f = 500MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 350W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 175MHz

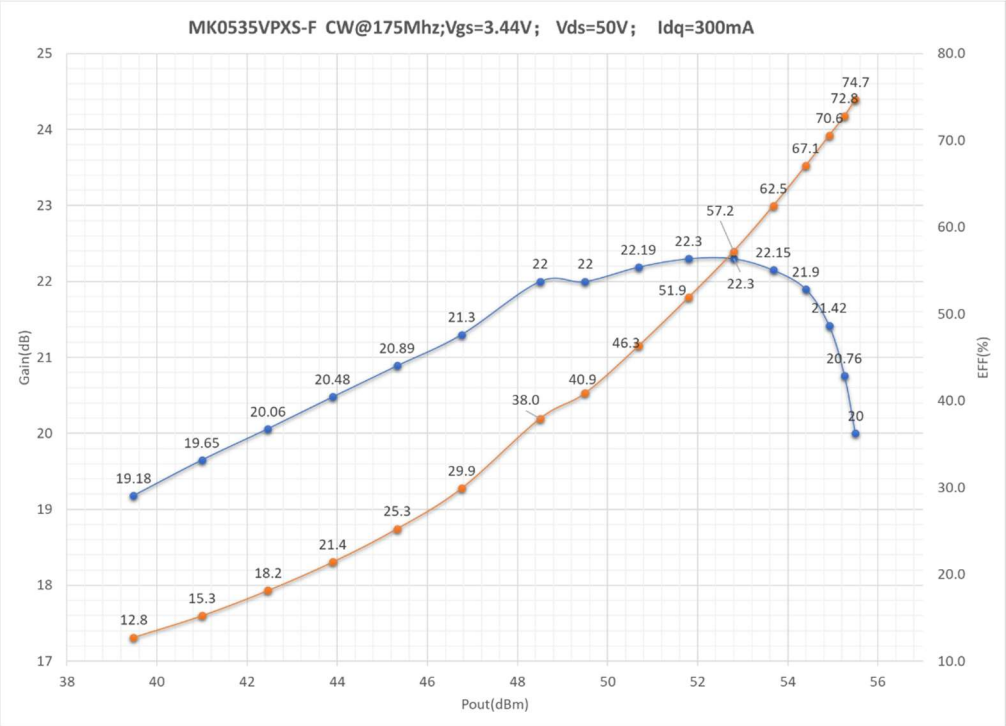
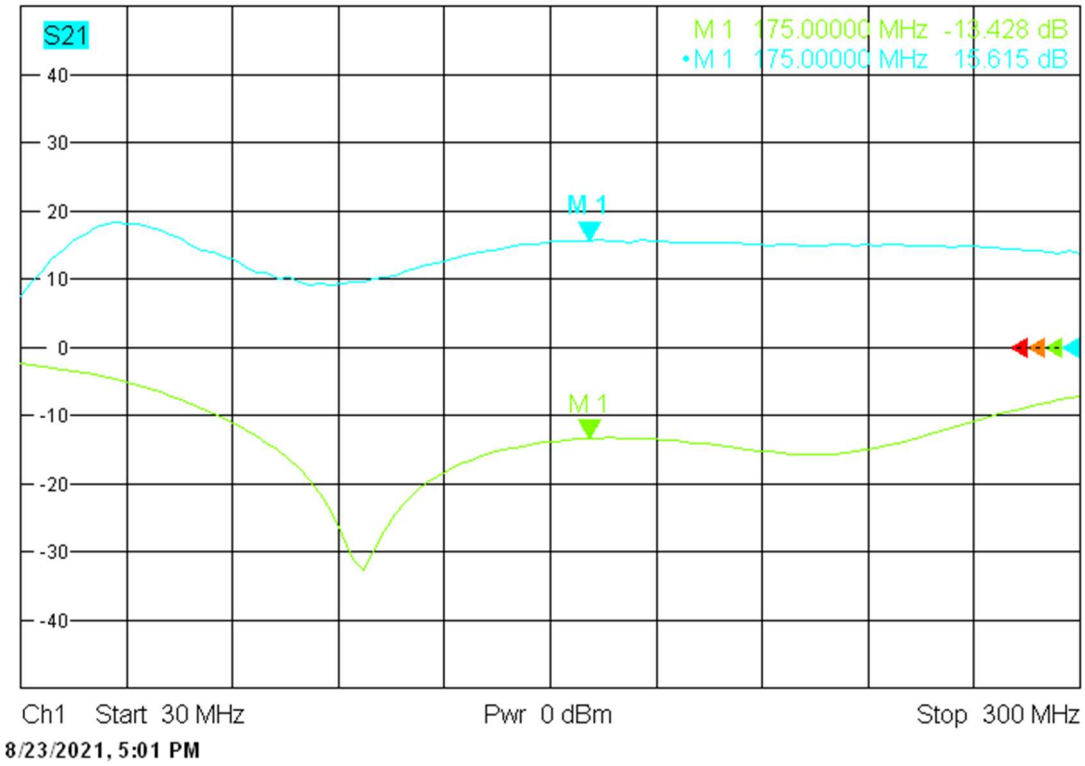


Figure 2: Network analyzer output S11/S21



Reference Circuit of Test Fixture Assembly Diagram (PCB file upon request)

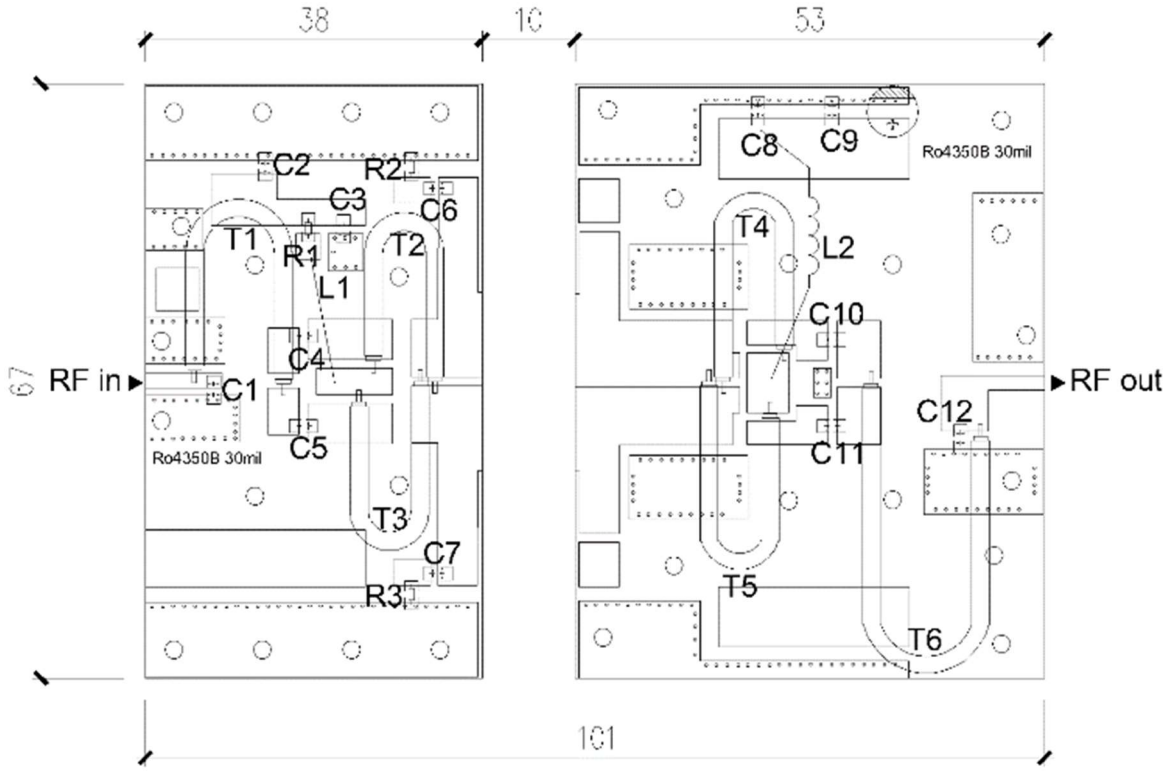


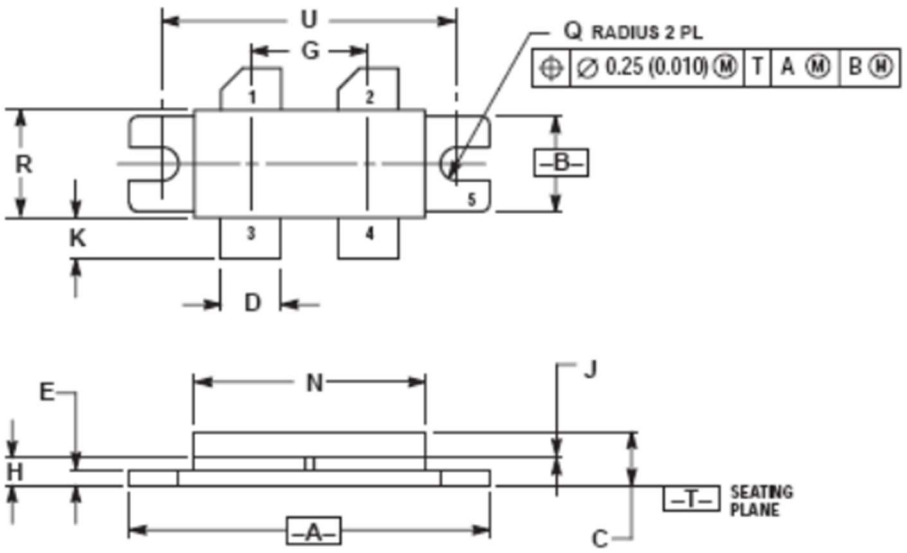
Table 1. Test Circuit Component Designations and Values (175MHz)

Component	Description	Suggested Manufacturer
C1	8.2pF	ATC800B
C2、C6、C7、C9	Ceramic multilayer capacitor, 10nF, 2KV	
C3、C4、C5、C8、C10、C11	1000pF	ATC800B
C12	2.2pF	ATC800B
R1	Chip Resistor,620Ω,1206	
R2、R3	Chip Resistor,9.1Ω,1206	
T1，T6	50Ω，80mm	
T2、T3	17Ω，48mm	
T4、T5	17Ω，80mm	
L1	直径 1mm，栅极馈电线	
L2	直径 1mm，绕径 5mm，6 圈	
PCB	30mil thickness,Ro4350B	

Package Outline

Flanged ceramic package;

Notice:MK0535VPXS(Earless) soldered on additional plated flange



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/8/23	Rev 1.0	Preliminary datasheet

Application data based on JF-21-10

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