



1GHz, 600W, 40V High Power RF LDMOS FETs

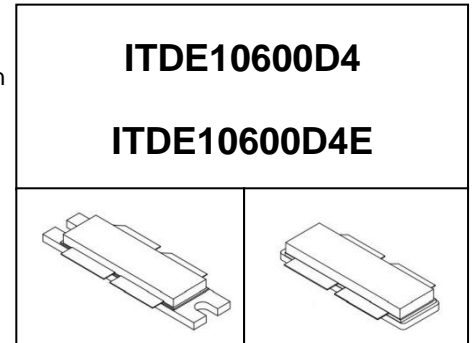
Description

The ITDE10600D4 is a 600-watt, internally matched LDMOS FETs, designed for Multiple ISM and RF Energy applications with frequencies up to 1GHz. It can be used in Class AB/B and Class C for both CW and pulse applications in narrowband operation

• Typical Performance (On Innogrator fixture with device soldered):

$V_{DD} = 40$ Volts, $I_{DQ} = 100$ mA, $T_{case} = 25$ degree C

Frequency	Signal	Gp (dB)	$P_{OUT}(W)$	$\eta_D @ P_{OUT}(\%)$
915MHz	CW	16.9	600	70.8



Recommended driver: MU1503V operated at 40V

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+42	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ C, T_J = 200^\circ C, DC$ test	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25$ C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)



Drain-Source Breakdown Voltage ($V_{GS}=0V$; $I_D=100\mu A$)	V_{DSS}	95	---	---	V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 40 V$, $V_{GS} = 0 V$)	I_{DSS}	---	---	10	μA
Gate--Source Leakage Current ($V_{GS} = 6 V$, $V_{DS} = 0 V$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 40V$, $I_D = 600 \mu A$)	$V_{GS(th)}$	---	2.0	---	V
Gate Quiescent Voltage ($V_{DD} = 40 V$, $I_{DQ} = 100 mA$, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.62	3.1	V

Functional Tests (On Innogrator Test Fixture, 50 ohm system) : $V_{DD} = 40 Vdc$, $I_{DQ} = 100 mA$, $f = 915 MHz$, $P_{in}=41dBm$ CW Signal Measurements.

Power Gain	G_p	---	16.5	---	dB
Drain Efficiency @ P_{OUT}	η_D	---	70	---	%
Output Power	P_{out}	---	600	---	W
Input Return Loss	IRL	---	-7	---	dB

Load Mismatch (In Innogrator Test Fixture, 50 ohm system): $V_{DD} = 40 Vdc$, $I_{DQ} = 100 mA$, $f = 915 MHz$

VSWR 10:1 at 600W Output Power at all Phase Angles, pulsed CW, 100us, 10%	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram
(Layout file upon request)

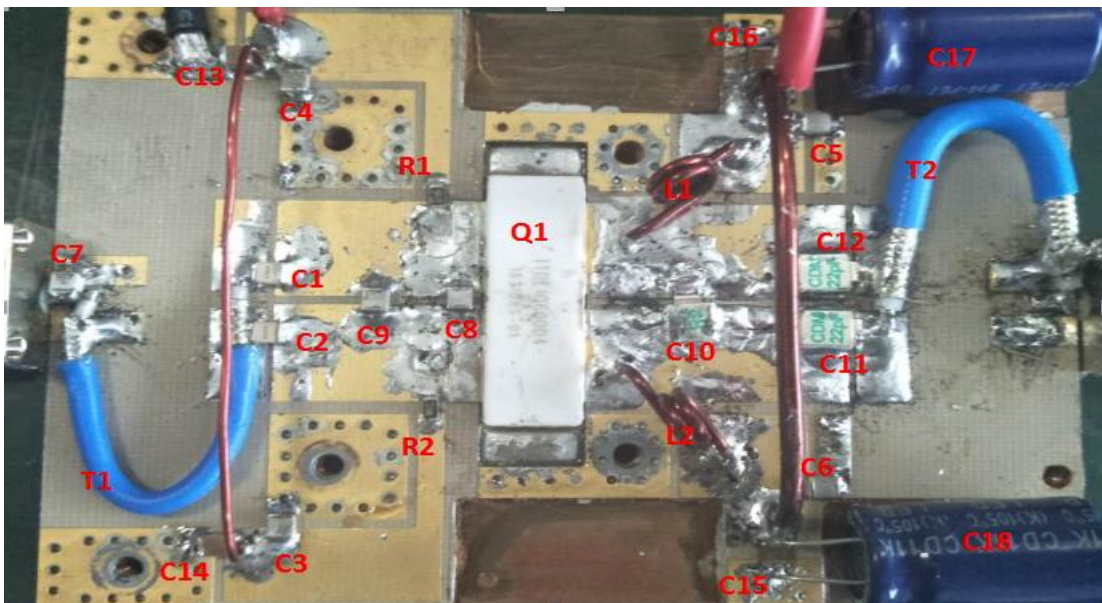




Table 5. Test Circuit Component Designations and Values

Part	description	model
C1~C6	33PF	ATC800B
C7	1PF	ATC800B
C8	8.2PF	ATC800B
R1,R2	9.1Ω	1206
C9	5.1PF	ATC800B
C10	15PF	MIN300VKITI/15PF
C11,C12	22PF	MIN300VKITI/22PF
C13,C14,C15,C16	10UF	100V/10UF
C17,C18	470UF	63V/470UF
T1	25Ω, line length =60mm	Φ2mm
T2	25Ω, line length =60mm	Φ3.6mm
Q1	ITDE10600D4	183108S-04
PCB	RF-35TC	30Mil

TYPICAL CHARACTERISTICS

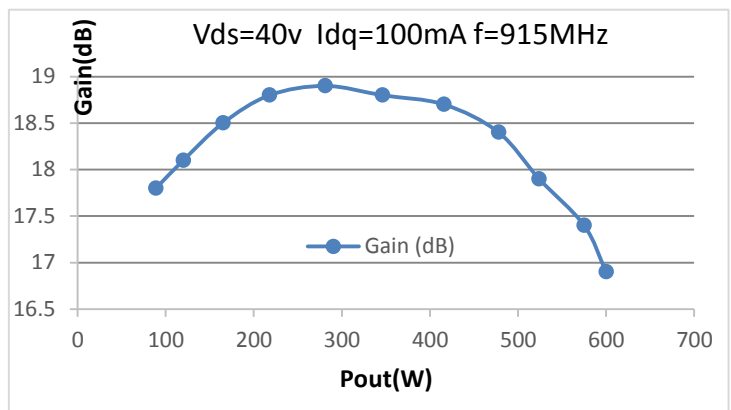
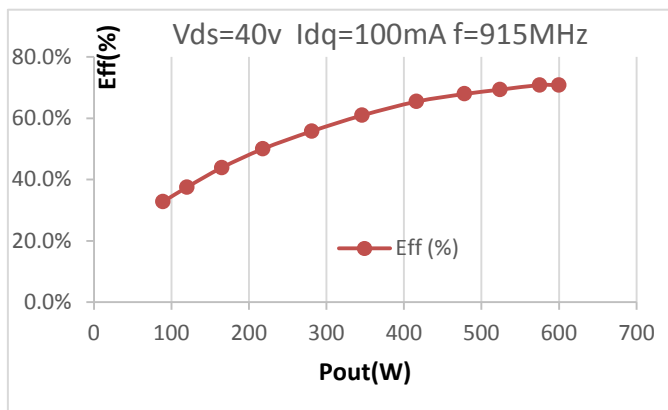
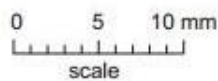
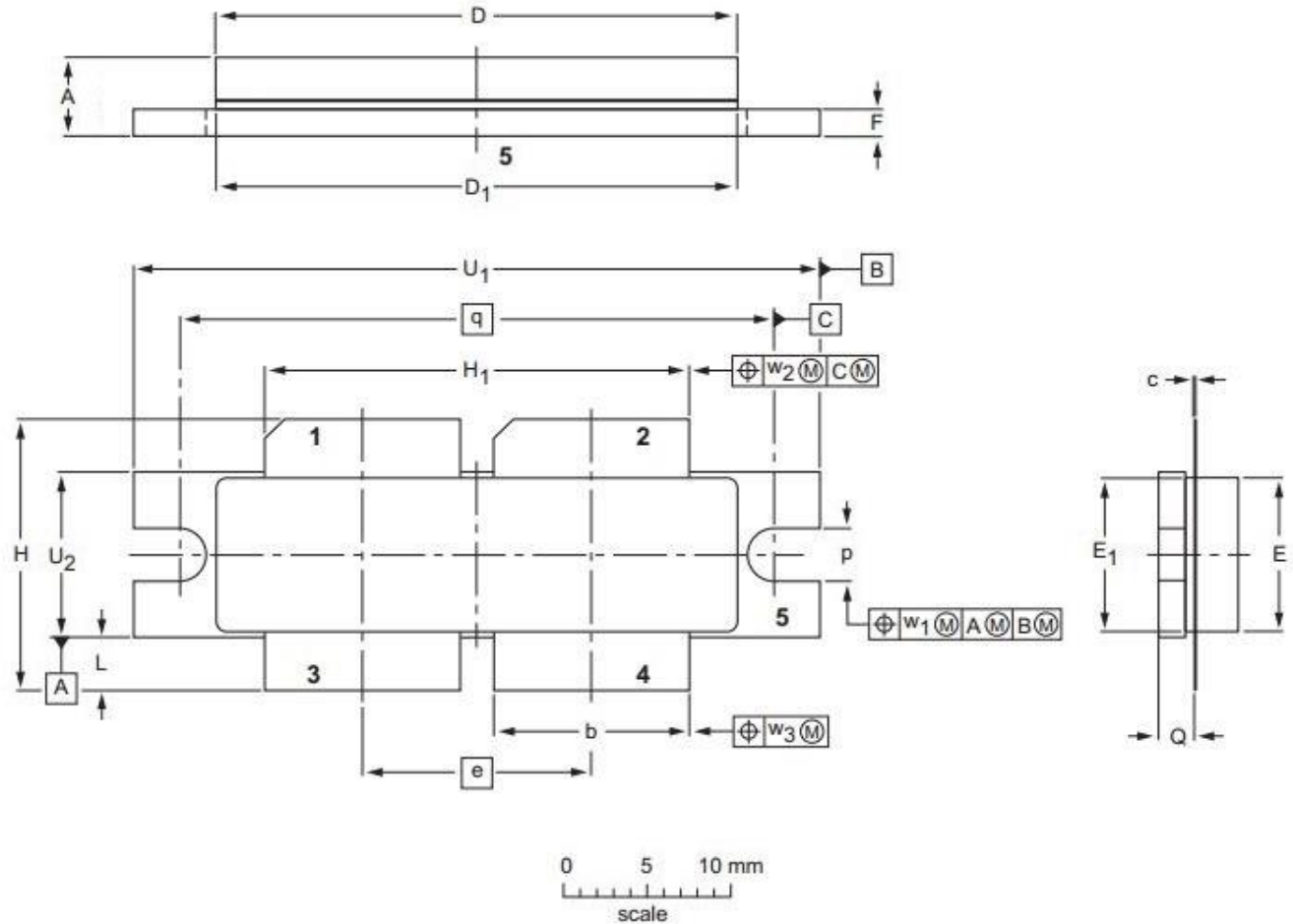


Figure 1. Drain Efficiency and Power Gain as Function of CW Output Power



Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)

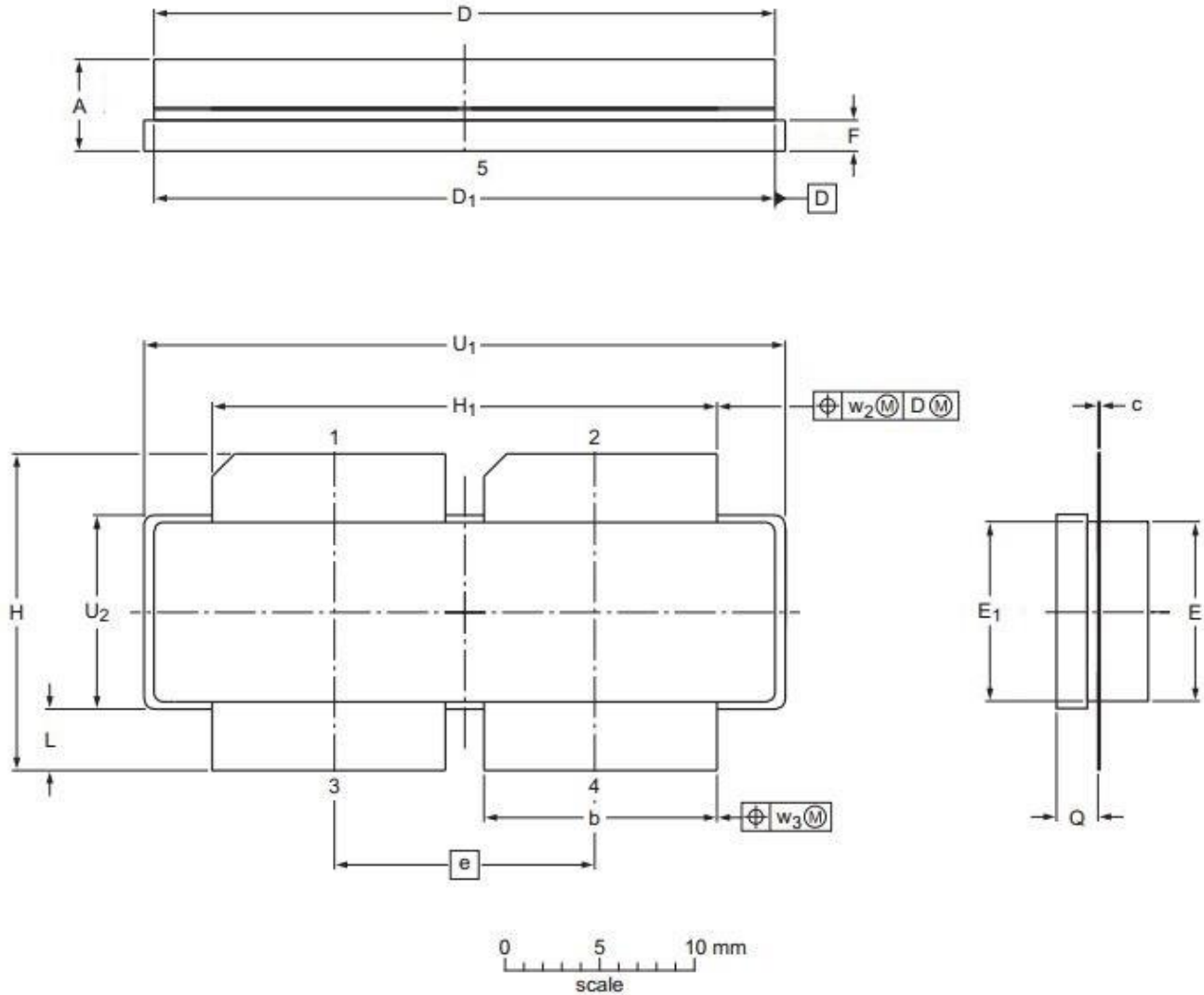


UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₃
mm	4.7	11.81	0.18	31.55	31.52		9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29			
	4.2	11.56	0.10	30.94	30.96	13.72	9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03	0.25	0.51	0.25
inches	0.185	0.465	0.007	1.242	1.241		0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405			
	0.165	0.455	0.004	1.218	1.219	0.540	0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013



Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2018/08/16	Rev 1.0	Preliminary Datasheet

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