MQ051K5VPX LDMOS TRANSISTOR

Document Number: MQ051K5VPX
Preliminary Datasheet V1.2

1500W, 50V High Power RF LDMOS FETs

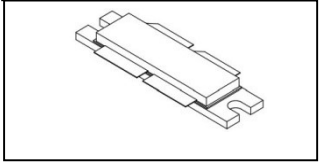
Description

The MQ051K5VPX is a 1500W capable, high performance, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 225MHz.

It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, HF communication, VHF TV and Aerospace applications.

MQ051K5VPX



- Typical Performance (On Innogration FM band fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 70 mA, CW,

Freq(MHz)	Pin(dBm)	Pout(W)	Gain(dB)	Eff(%)
88	44.1	1420	17.4	83%
98	45.7	1600	16.3	85%
108	46	1700	16.5	86%

- Typical Performance (On Innogration narrowband fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 200 mA, Pulsed CW：100us，10%

Freq(MHz)	Pin(dBm)	Pout(W)	Gain(dB)	Eff(%)
13.56	36	1560	26	83.81

Features

- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 1500W CW, 50 Vdc, I_{DQ} = 70 mA	$R_{\theta JC}$	0.09	°C/W
Transient thermal impedance from junction to case	Zth	0.02	°C/W

Tj = 150° C; tp = 100 us; Duty cycle = 20 %			

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS}(th)$	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 70 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		72		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		520		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		143		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.4		pF

TYPICAL CHARACTERISTICS

88-108MHz

Figure 2: Gain and Power Efficiency as a Function of Pout

Vds = 50 V, Idq = 70 mA,

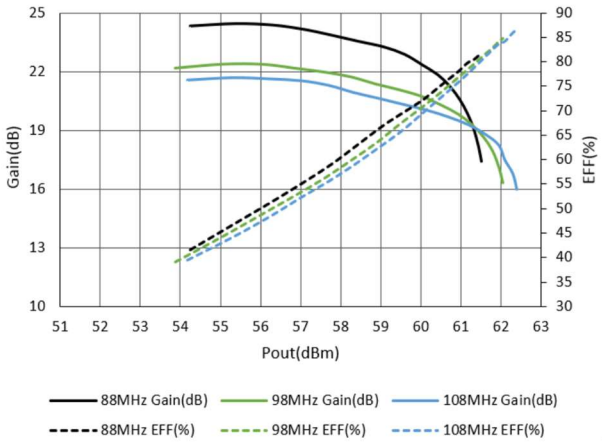
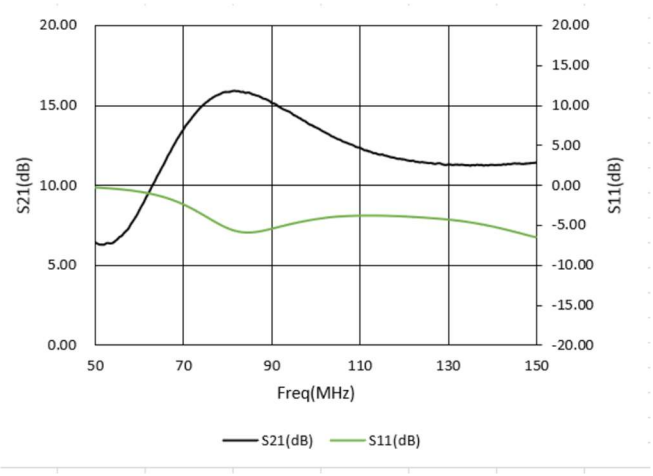


Figure 2: Network analyzer output S11/S21

Vds = 50 V, Idq = 500 mA,



13.56MHz

Figure 3: Gain and Power Efficiency as a Function of Pout

Vds = 50 V, Idq = 200 mA,

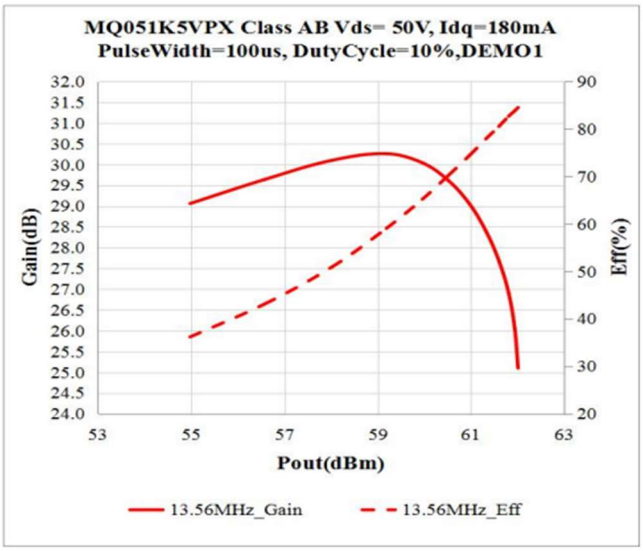
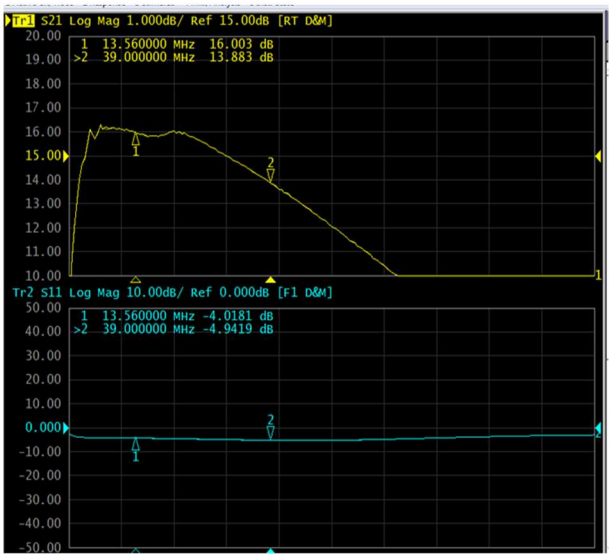


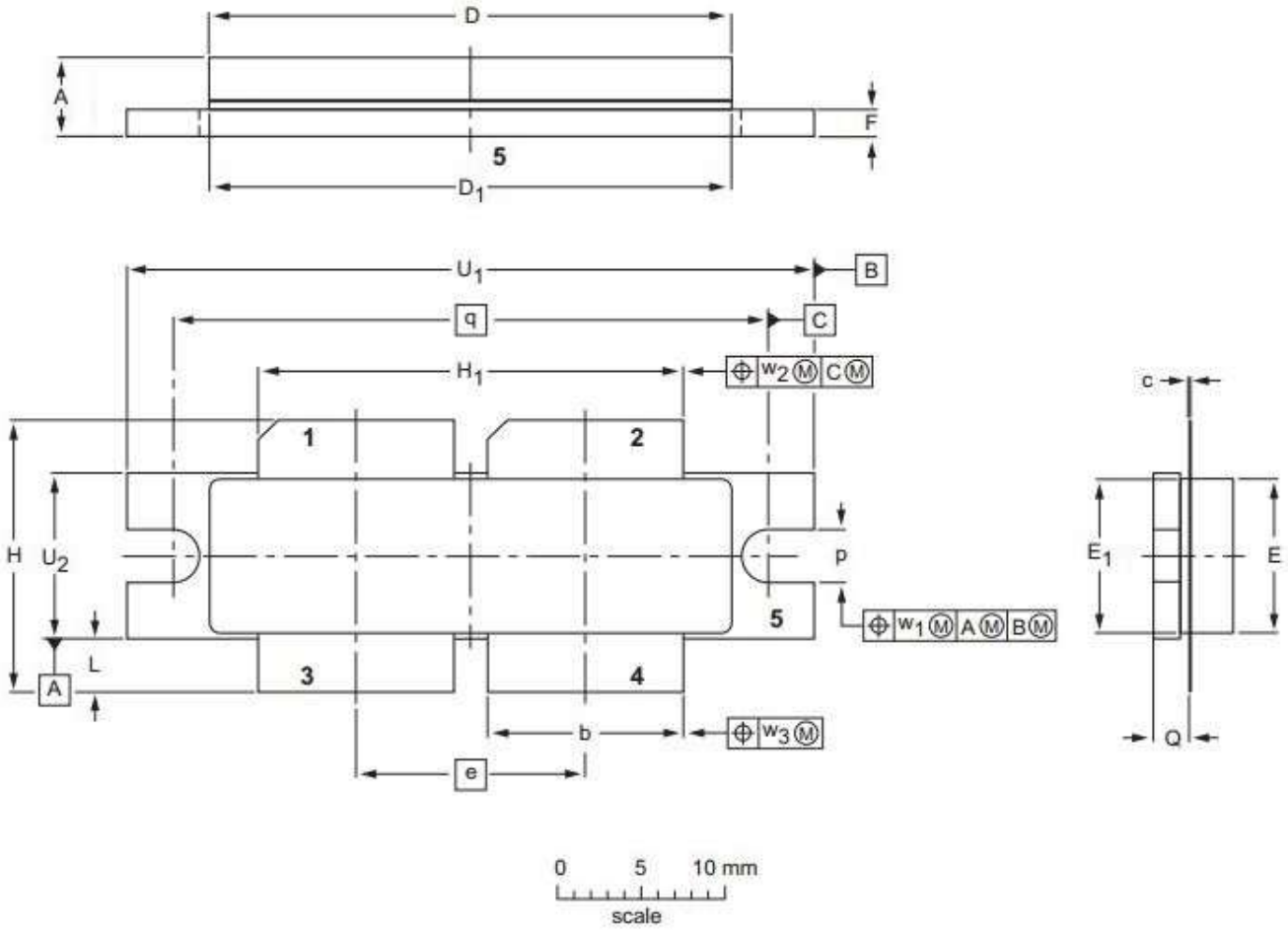
Figure 4: Network analyzer output S11/S21

Vds = 50 V, Idq = 500 mA,



Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2020/4/13	Rev 1.0	Preliminary Datasheet
2020/4/17	Rev 1.1	Update on capacitance
2021/9/22	Rev 1.2	Update based on latest 13.56MHz app data

Application data based on GZY-20-15, HL-21-34

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