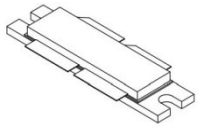
MQ051K0RVP LDMOS TRANSISTOR

Document Number: MQ051K0RVP
Preliminary Datasheet V1.1

1000W, 0.2-0.5GHz 50V High Power RF LDMOS FETs

MQ051K0RVP



Description

The MQ051K0RVP is a 1000W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications from 200MHz up to 500MHz, supporting both pulse and CW applications.

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as VHF communication, UHF TV and Aerospace applications.

There isn't guarantee when this device is used outside of the band stated above.

- Application data at 325MHz with device soldered,
  CW signal, Vgs=3.2V,Vds=50V, Idq=250mA

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	Eff(%)
325	39.38	60.51	1124.6	30.43	21.13	73.91
	40.28	60.66	1164.1	31.06	20.38	74.96
	41.22	60.81	1205.0	31.80	19.59	75.79

Recommended driver:MU1503V

Features

- High breakdown voltage enable high ruggedness
- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 800W CW, 50 Vdc, I_{DQ} = 340 mA	$R_{\theta JC}$	0.15	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0mA	$V_{(BR)DSS}$		115		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 340 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.2	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		41		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		286		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		110		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		2.5		pF

TYPICAL CHARACTERISTICS (325MHz)

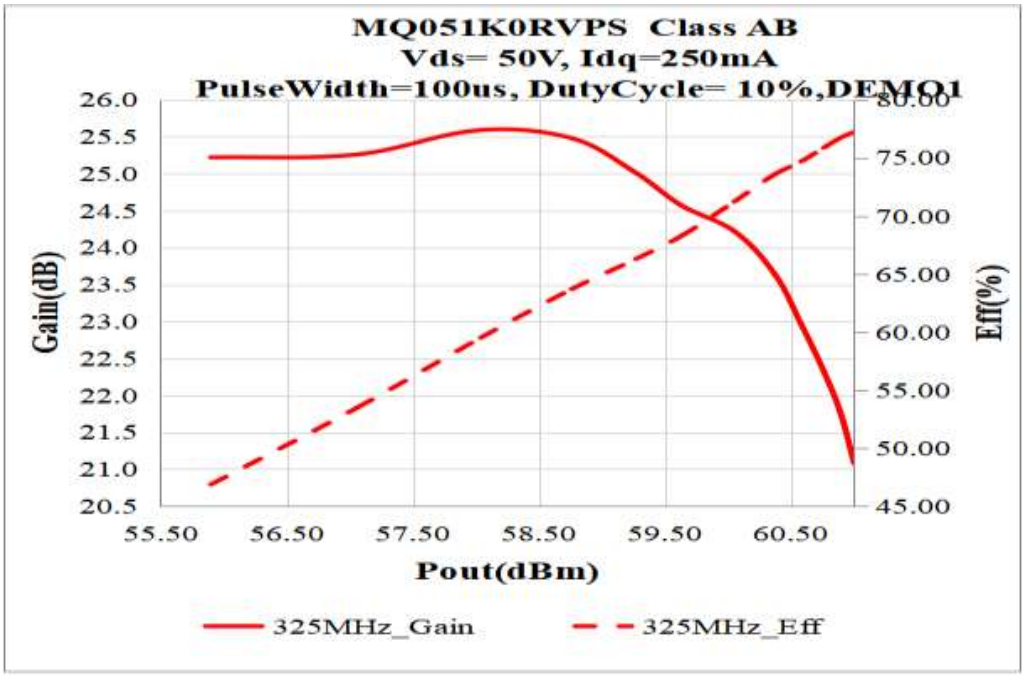


Figure 1: Efficiency and power gain as the function of Pout (Vds=50V, Idq=250mA,CW)

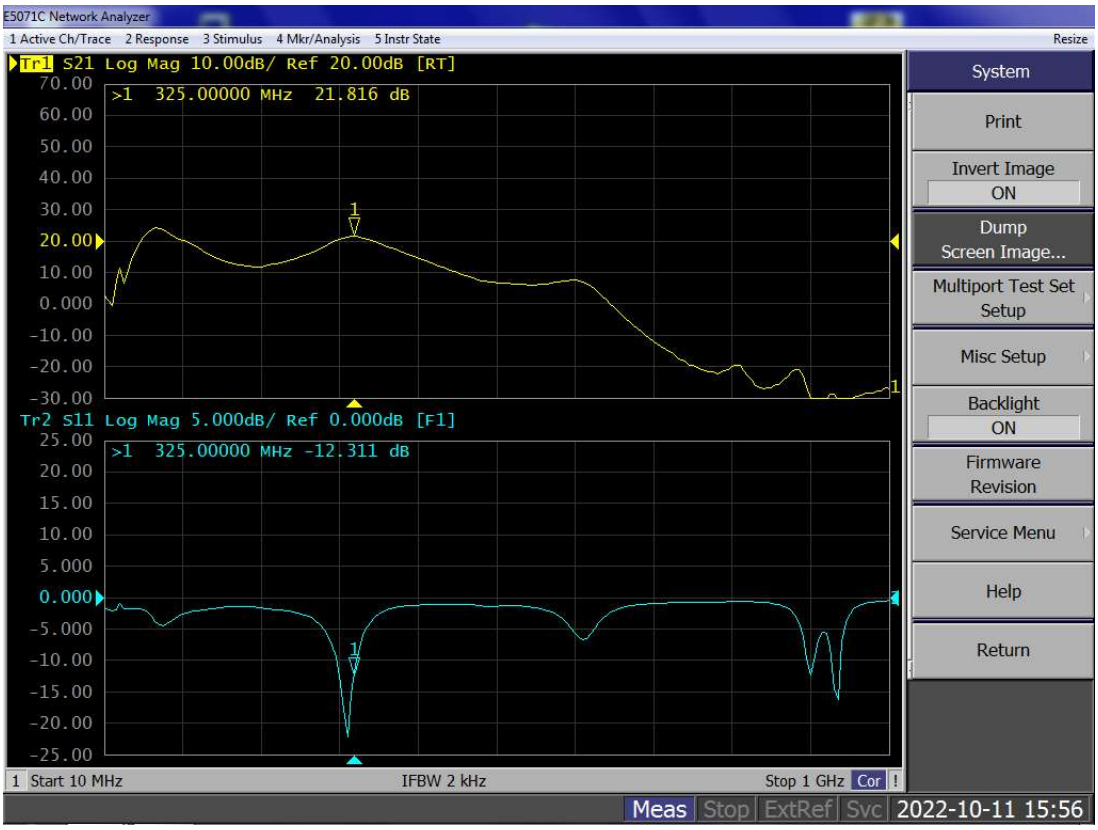
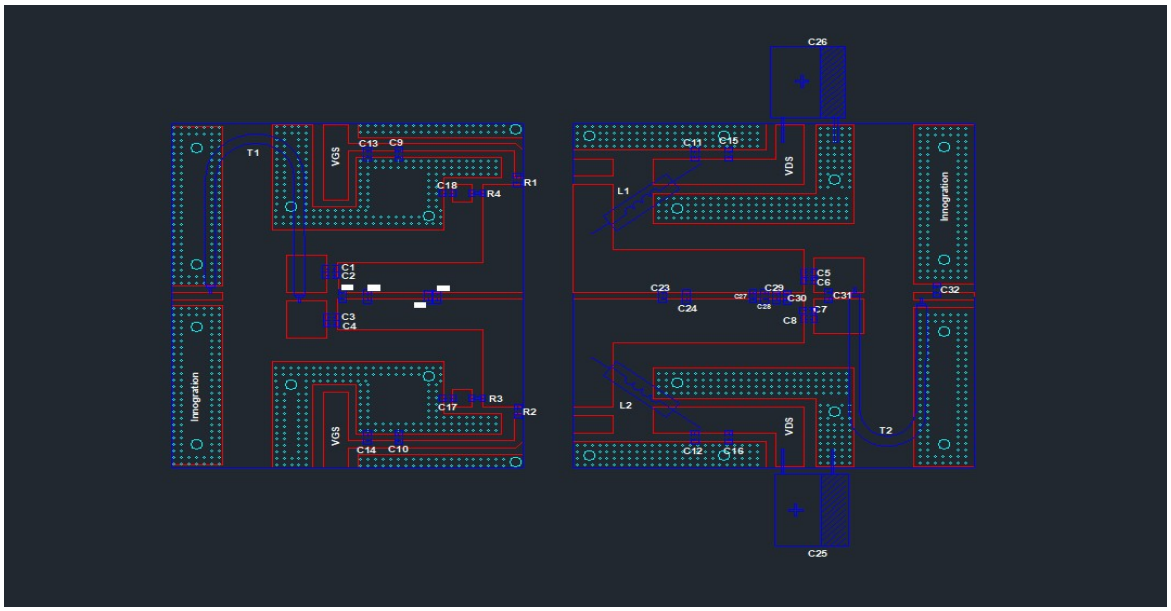


Figure 2: Network analyzer output, S11 (Vds=50V,Idq=1400mA, Vgs=3.35V)

Reference Circuit of Test Fixture (325MHz)

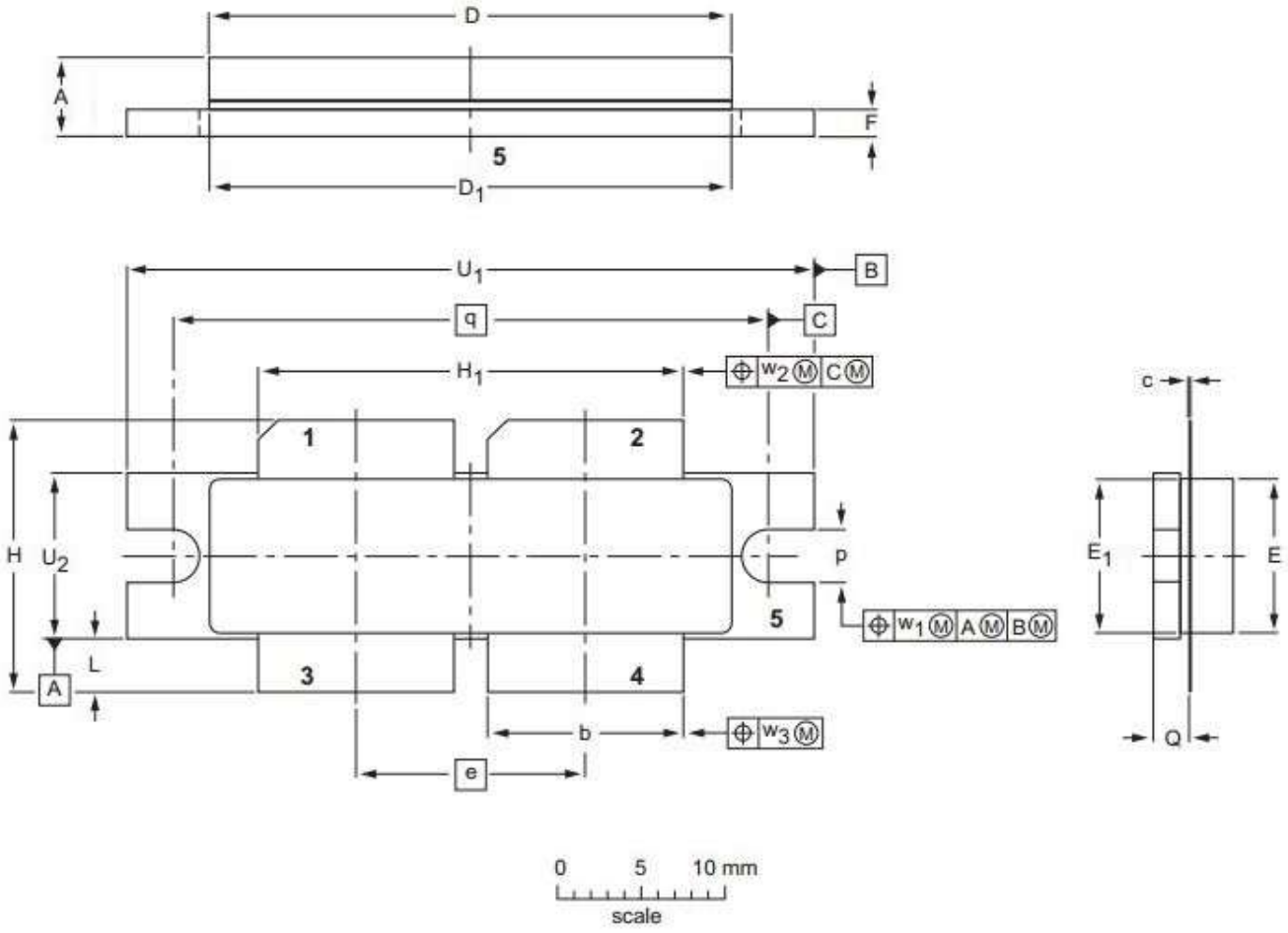
(Layout file upon request) PCB: Roger 4350B, 30mils



Part	description	Model
C1~C12	200pF	Beijing YN MQ101111
C13~C16	10nF	Ceramic multilayer capacitor
C17,C18	220pF	Beijing YN MQ101111
C19	22pF	Beijing YN MQ101111
C20,C21,C22	20pF	Beijing YN MQ101111
C23,C28	8.2pF	Beijing YN MQ101111
C24	5.6pF	Beijing YN MQ101111
C27	3.3pF	Beijing YN MQ101111
C29,C30	10pF	Beijing YN MQ101111
C31	4.7pF	Beijing YN MQ101111
C32	2pF	Beijing YN MQ101111
C25,C26	4700uF/63V	Electrolytic Capacitor
R1,R2,R3,R4	10Ω	Chip Resistor
T1	25ohm/50mm	
T2	25ohm/60mm	
L1，L2	3turns,D=5mm　D=1mm	DIY air core inductance
PCB	0.762mm [0.030''] thick, εr=3.50, Rogers 4350B, 1 oz. copper	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/10/18	Rev 1.0	Preliminary Datasheet
2022/10/11	Rev 1.1	Modify according to the latest application report

Application data based on TC-22-07

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