MG1707S LDMOS TRANSISTOR

Document Number: MG1707S Product Datasheet V2.0

70W, L band 28V High Power RF LDMOS FETs

Description

The MG1707S is a 70-watt, internally matched, single ended LDMOS FETs, designed for multiple applications within 1.1-1.7GHz. It can be used in Class AB/B and Class C for all typical modulation formats, for CW and pulsed, linear or saturated applications.

Typical Performance (On Innogration fixture with device soldered):
 V_{DD} = 28Volts, I_{DQ} = 150 mA, CW

755 20 Fello, 150 Fello III I, 611					
F(MHz)	Pin (dBm)	Pout (W)	ld(A)	Gain (dB)	Eff(%)
1100	37.1	80.5	5.1	12.0	56.8
1200	37.7	79.4	5.5	11.3	51.6
1300	36.7	81.3	5.8	12.4	50.1
1400	37.7	83.2	6.4	11.5	46.4
1500	37.5	89.1	6.8	12.0	46.8
1600	37.7	89.1	6.7	11.8	47.5
1700	37.4	82.2	6.2	11.8	47.5

MG1707S

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- · L band amplifier
- · ISM applications
- GPS, Beidou power amplifier

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	+65	Vdc
GateSource Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	$V_{\scriptscriptstyle DD}$	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	T₃	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Do 10	0.0	°C/W
T _C = 85°C, T _J =200°C, DC test	Rejc	0.9	-C/VV

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

VSWR 10:1 at 70W pulse CW Output Power

Characteristic	Symbol	Min	Тур	Max	Unit
OC Characteristics					
Zero Gate Voltage Drain Leakage Current				100	
$(V_{DS} = 65V, V_{GS} = 0 V)$	I _{DSS}			100	μΑ
Zero Gate Voltage Drain Leakage Current				4	
$(V_{DS} = 28 \text{ V}, V_{GS} = 0 \text{ V})$	I _{DSS}				μΑ
GateSource Leakage Current	I _{GSS}			1	μА
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$					
Gate Threshold Voltage	V (II)		2.0		.,
$(V_{DS} = 28V, I_D = 450 \mu A)$	V _{GS} (th)				V
Gate Quiescent Voltage		1	2.67		V
$(V_{DD}$ = 28 V, I_{D} = 150 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.67		
Functional Tests (On Demo Test Fixture, 50 ohm system) V _{DD} = 28 V	'dc, I _{DQ} = 150 mA	, f = 1100 MH	z, Pulse CW S	ignal Measure	ments.
Power Gain	Gp		12		dB
Drain Efficiency@P3dB	η _D		55		%
3 dB Compression Point	P _{-3dB}	70			W

TYPICAL CHARACTERISTICS

No Device Degradation

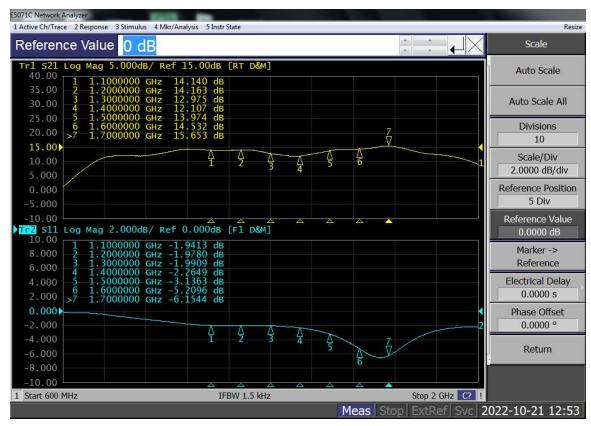
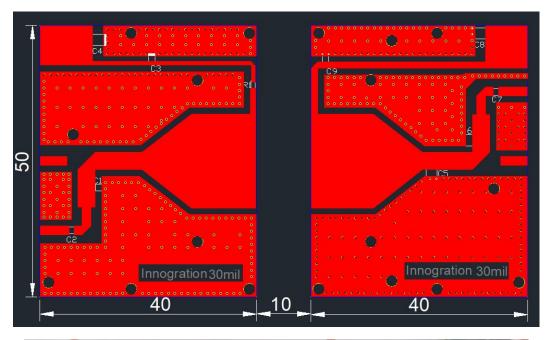


Figure 2. Network analyzer output S11/S21 (VDS=28V IDQ=150mA VGS=2.67V)

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Figure 3. Test Circuit Component Layout



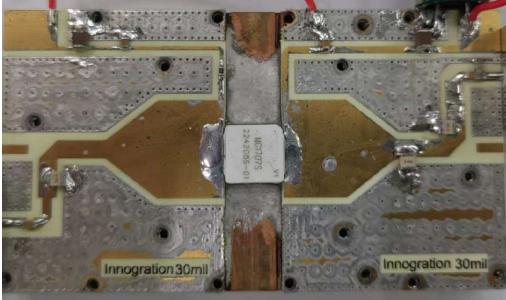
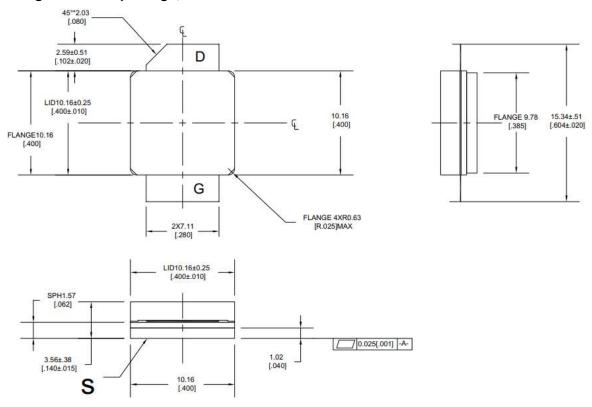


Table 4. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C2、C3、C7、C9	56pF ATC 100A	
C1	1.8pF ATC 100B	
C6、C5	1pF ATC 100B	
C4、C8	10UF 1210	
R1	8.2'Ω 0603	
PCB	30mil Rogers4350B	

Package Outline

Earless flanged ceramic package; 2 leads



Unit: mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/8/26	Rev 1.0	Product Datasheet
2022/10/21	Rev 2.0	Update according to V1 new design

Application data based on SYX-22-20

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