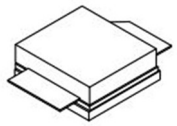
MG2004S LDMOS TRANSISTOR

Document Number: MG2004S
Product Datasheet V1.0

40W, L band 1-2GHz 28V RF LDMOS FETs

MG2004S



Description

The MG2004S is a 40-watt, internally matched, single ended LDMOS FETs, designed for multiple applications within full band 1.0-2.0GHz.

It can be used in Class AB/B and Class C for all typical modulation formats, for CW and pulsed, linear or saturated applications.

- Typical Performance (On Innogration fixture with device soldered):

  V_{DD} = 28Volts, I_{DQ} = 200 mA, CW

F(MHz)	Pin（dBm）	Pout（W）	I(A)	Gain（dB）	Eff(%)
1000	36.0	56.2	4.7	11.5	43.0
1100	36.0	52.1	4.5	11.2	41.4
1200	35.0	55.8	4.5	12.5	44.6
1300	35.0	58.2	4.2	12.7	49.4
1400	35.7	55.7	3.7	11.8	53.8
1500	34.8	54.6	3.5	12.6	55.1
1600	35.9	52.5	3.5	11.3	53.1
1700	34.7	57.5	3.8	12.9	54.5
1800	34.7	57.1	3.9	12.9	52.9
1900	34.8	56.2	4.1	12.7	48.7
2000	35.3	49.0	4.0	11.6	43.7

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- L band amplifier
- ISM applications
- GPS, Beidou power amplifier

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.6	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 450 μA)	$V_{GS(th)}$		2.0		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.95		V
Functional Tests (On Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 200 mA, f = 1000 -2000MHz, Pulse CW Signal .					
Power Gain	Gp	11	12		dB
Drain Efficiency@P3dB	η_D		55		%
3 dB Compression Point	P_{-3dB}	40			W
Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 200 mA, f = 2000 MHz					
VSWR 5:1 at 70W pulse CW Output Power	No Device Degradation				

TYPICAL CHARACTERISTICS

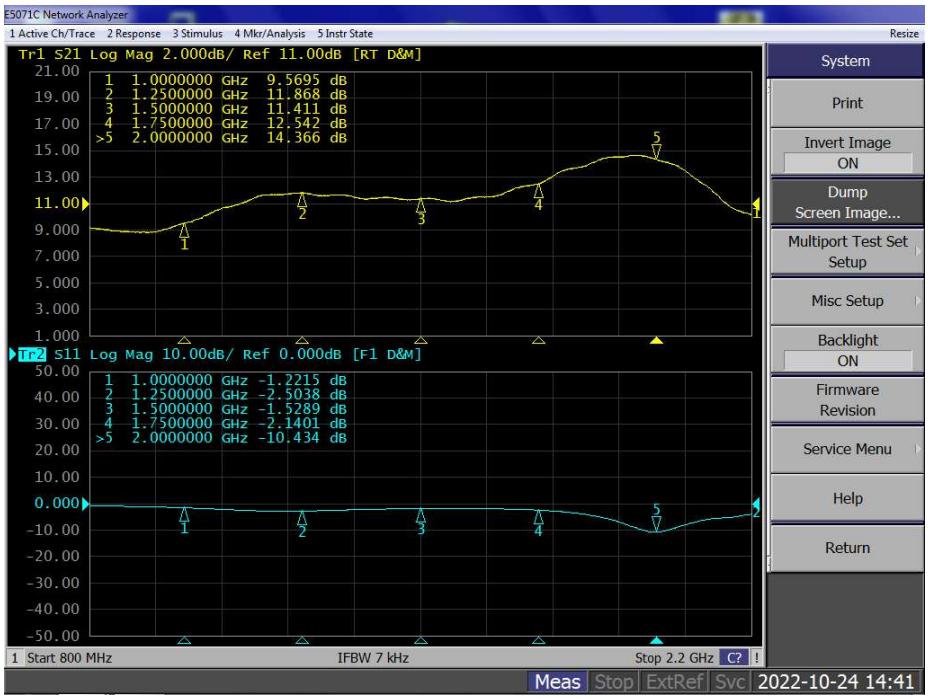
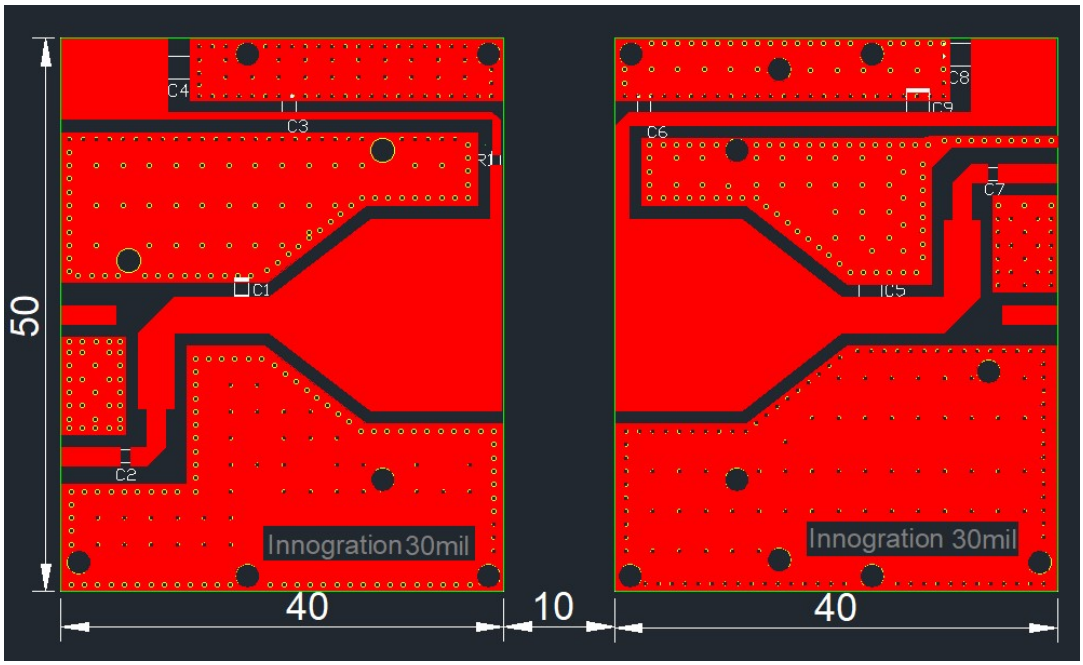


Figure 2. Network analyzer output S11/S21 (VDS=28V IDQ=200mA VGS=2.95V)

Figure 3. Test Circuit Component Layout



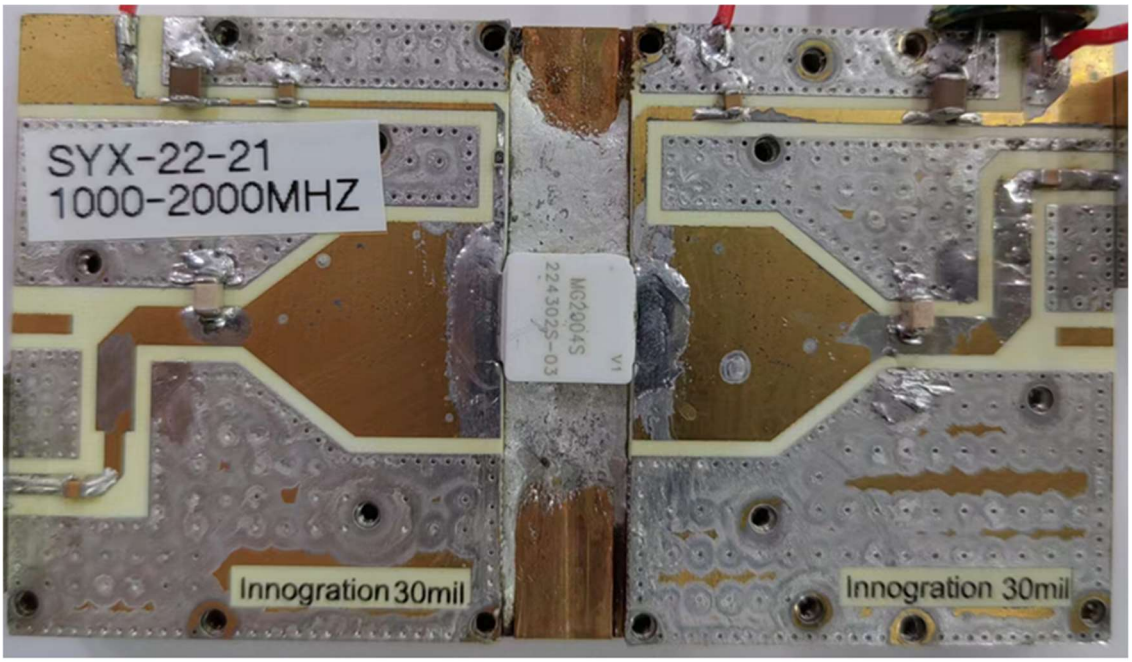
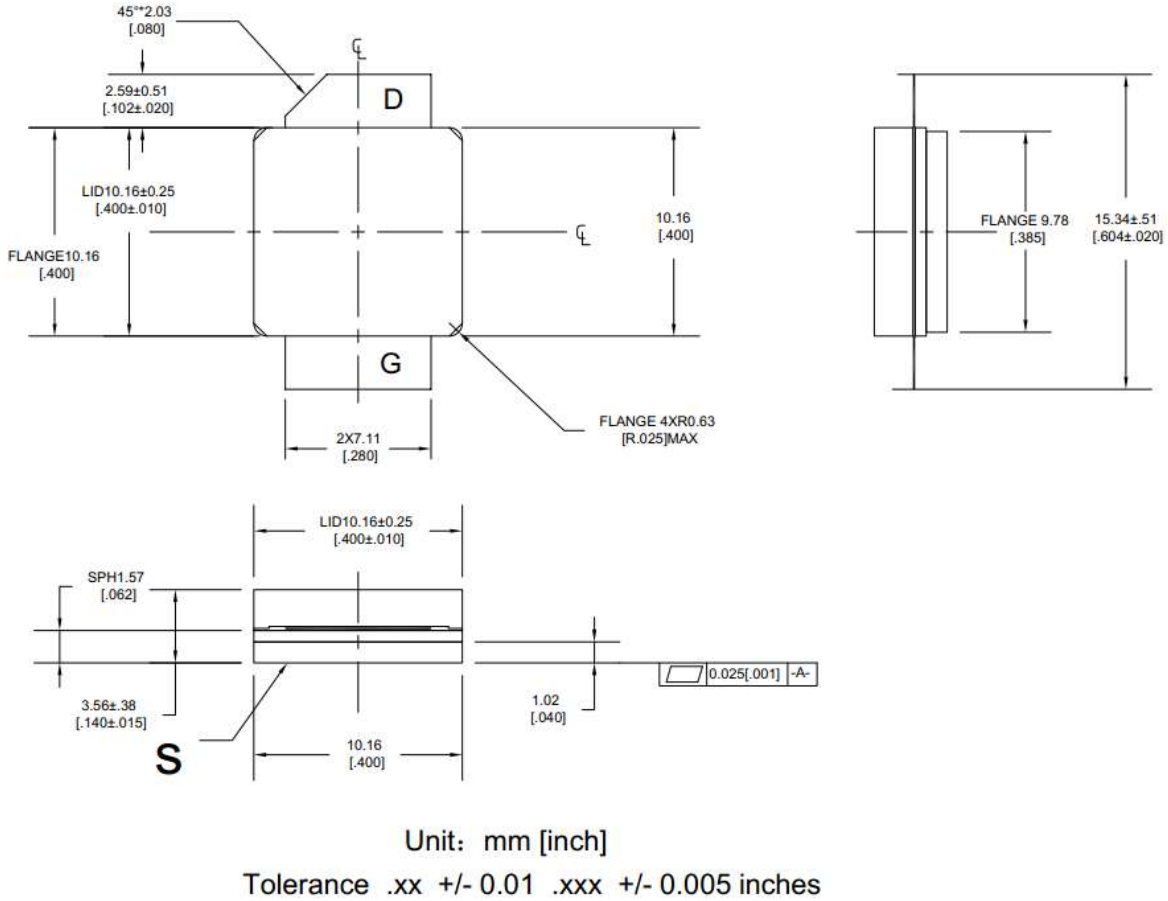


Table 4. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C2、C3、C7、C6	56pF ATC 100A	
C1	2.0pF ATC 100B	
C5	1.0pF ATC 100B	
C4、C9	10UF 1210	
C8	63V 470UF	
R1	7.5Ω 0603	
PCB	30mil Rogers4350B	

Package Outline

Earless flanged ceramic package; 2 leads



Unit: mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/10/24	**Rev 1.0**	**Product Datasheet**

Application data based on SYX-22-21

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