



Gallium Nitride 50V, 700W,0.6-1GHz RF Power Transistor

Description

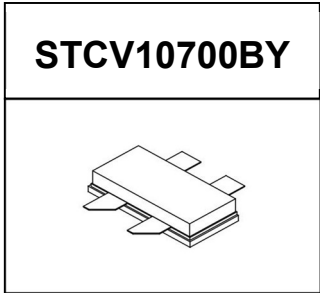
The STCV10700BY4 is a dual path 700watt capable, GaN HEMT, ideal for applications from 0.6 to 1GHz.

It can support CW, pulse or any modulated signal. It can be configured as push pull or Doherty.

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical Pulse CW performance on 758-803MHz Doherty

$V_{DD} = 50 \text{ Vdc}$, $I_{DQ} = 280\text{mA}$, $V_{gs_main} = -3.1\text{V}$, $V_{gs_peak} = -5.6\text{V}$, 20us 10%



Freq (MHz)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)	P3dB Gain(dB)	P5dB (dBm)	P5dB (W)	P5dB Eff(%)
758	58.35	683.1	77.7	16.0	58.98	791.6	79.3
780	58.4	691.1	79.6	17.0	58.9	776.0	81.2
803	58.19	658.7	80.0	17.4	58.54	714.9	81.8

Typical WCDMA 1 carrier performance

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Efficiency (%)
758	50.50	8.92	59.42	874.0	-25.8	17.2	62.1
780	50.50	8.96	59.46	882.2	-26.7	18.0	62.2
803	50.50	8.65	59.15	821.6	-25.1	18.5	61.3

Applications

- Asymmetrical Doherty amplifier within 0.6-1GHz
- UHF TV
- P band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

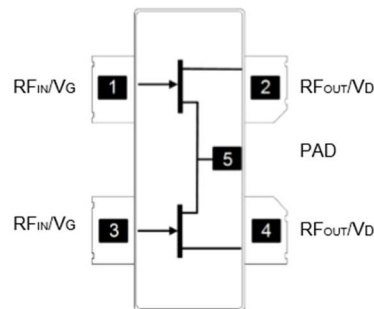




Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	94	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c= 25^{\circ}C$, at $P_d=90W$, on Doherty application board	$R_{\theta JC}$	1.2	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8V$; $I_{DS}=39.6mA$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} =10V$, $I_D = 39.6mA$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} =50V$, $I_{DS}=220mA$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8V$; $I_{DS}=54mA$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} =10V$, $I_D = 54mA$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} =50V$, $I_{DS}=300mA$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	800MHz, $P_{out}=110W$ WCDMA 1 Carrier output All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

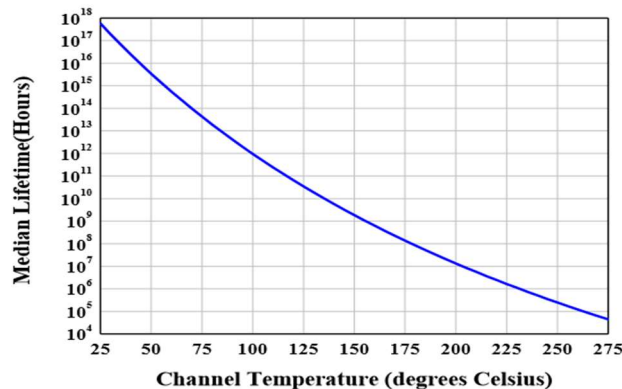




Figure 3: Efficiency and power gain as function of Pout (758-803MHz Doherty)

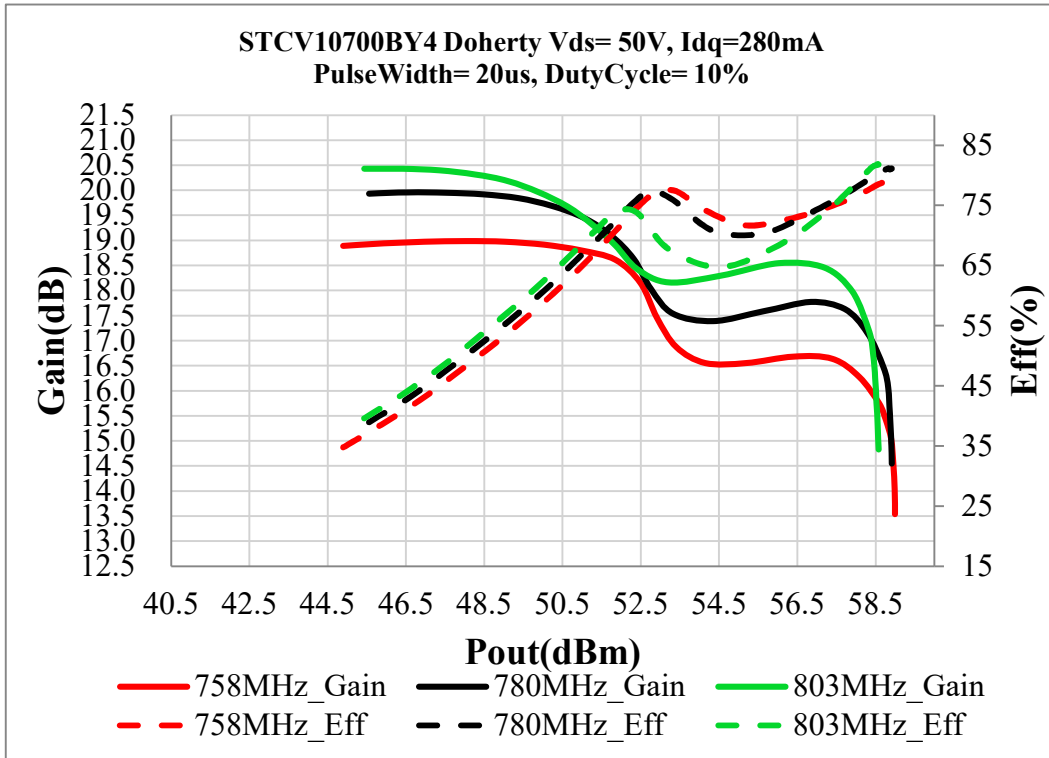


Figure 4: Network analyzer output, S11 and S21 (758-803MHz Doherty)

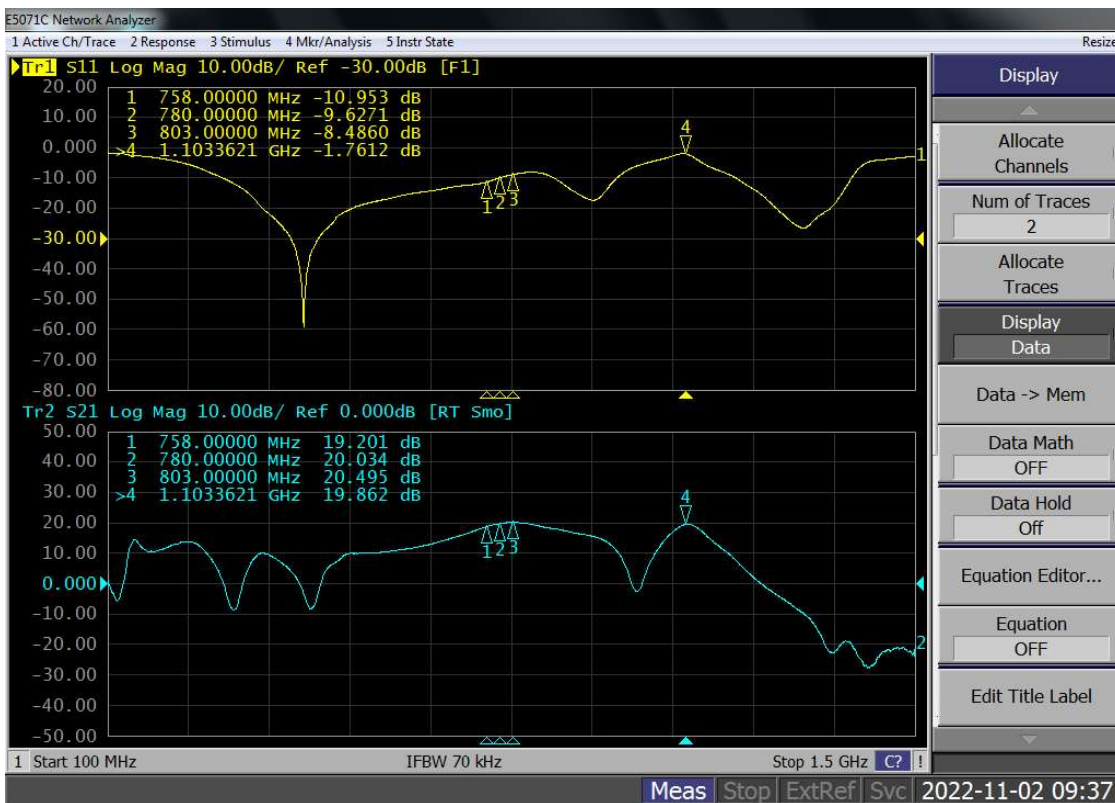


Figure 5: Picture of application board Doherty circuit for 758-803MHz

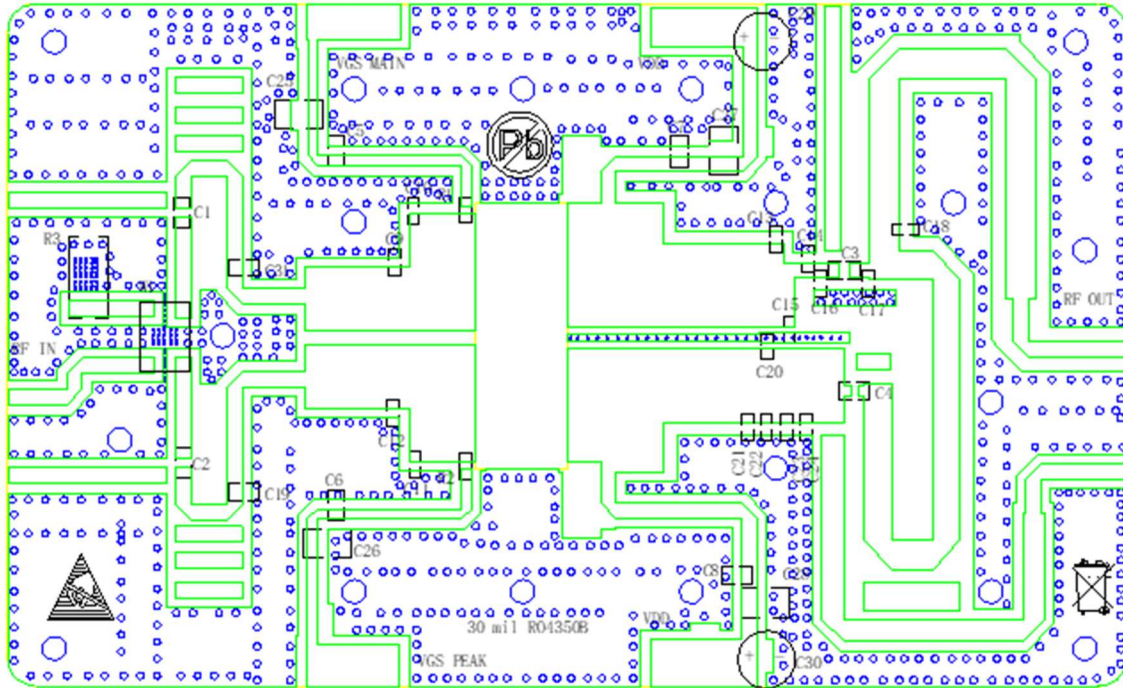
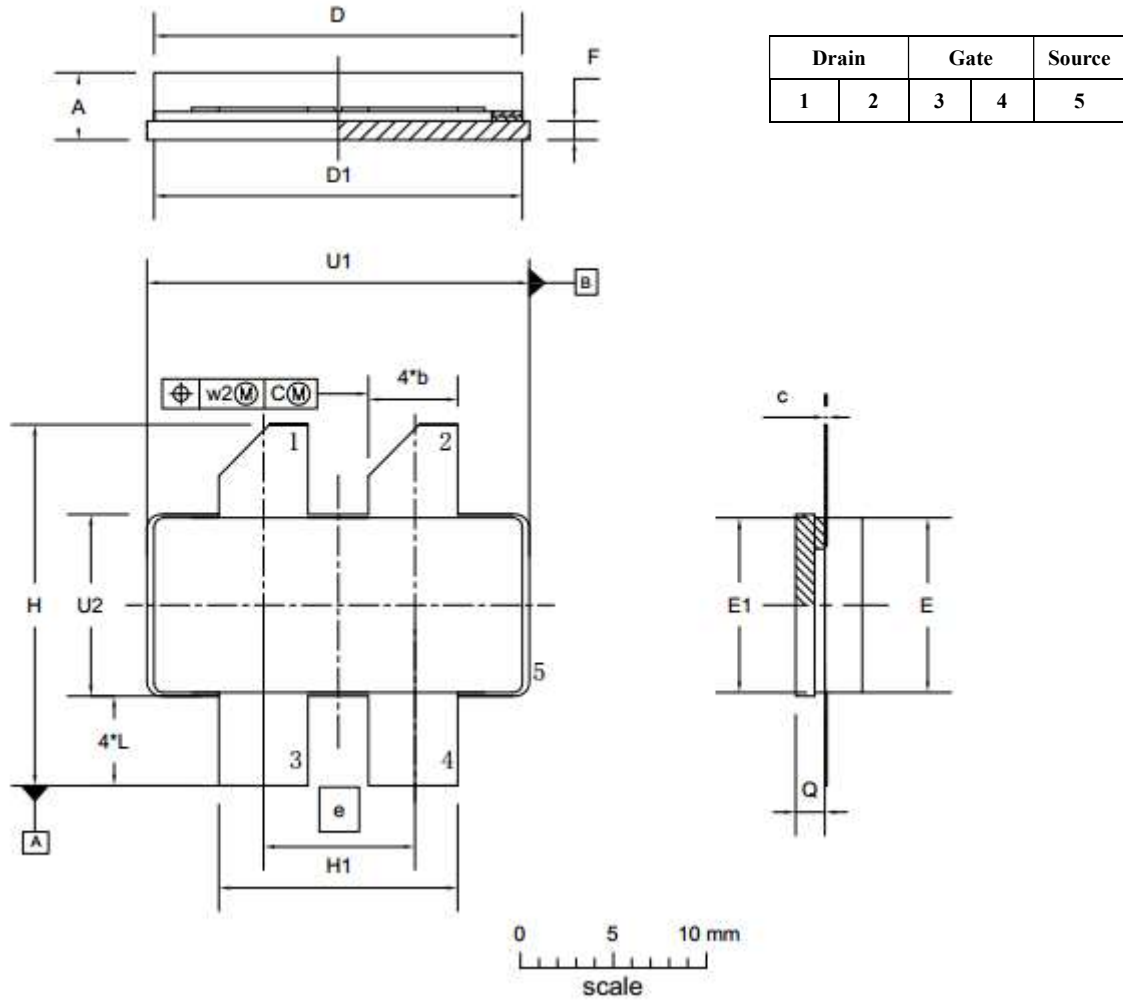


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 30mils)

Designator	Footprint	Comment	Quantity
C1, C2, C3, C4, C5, C6, C7, C8	0805	68pF	8
C9, C11, C12	0603	6.8pF	3
C10	0603	8.2pF	1
C13	0603	4.7pF	1
C14, C15, C16, C20, C21, C22, C23	0603	3.3 pF	7
C17, C24	0603	2.0	2
C18, C19, C31	0603	1.0pF	3
C25, C26, C27, C28	1210	10uF/100V	4
C29, C30		100uF/63V	2
R1, R2	0603	10R	2
R3	2512	51R	1
W1		DC07F02	1



Earless Flanged Ceramic Package; 4 leads



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₁	W ₂
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	1.70	20.70	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	1.45	20.45	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.067	0.815	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.057	0.805	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/4/1	V1.0	Preliminary Datasheet Creation
2022/11/2	V2.0	Application result updated

Application data based on: LSM-22-05

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