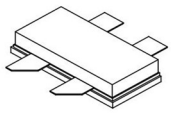
GaN HEMT 50V, 350W,2.3-2.7GHz RF Power Transistor

STBV27350BY4



Description

The STBV27350BY4 is a dual path 350watt, Input matched GaN HEMT, ideal for applications from 2.3 to 2.7GHz especially for LTE/5G

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical WCDMA 1 carrier performance on **2.5-2.7GHz** asymmetrical Doherty with device soldered

VDS= 50V, IDQ=300mA(Vgm=-3.02V，Vgp=-5.6V

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Efficiency (%)
2500	47.5	7.26	-26.90	16.00	53.72
2600	47.5	7.59	-27.27	15.76	56.60
2700	47.5	7.38	-26.84	14.06	53.12

- Typical WCDMA 1 carrier performance on **2.3-2.4GHz** asymmetrical Doherty with device soldered

VDS= 50V, IDQ=100mA(Vgm=-3.18V，Vgp=-6.0V)

Freq (MHz)	Pout (dBm)	CCDF (dB)	ACPR (dBc)	Gain (dB)	Efficiency (%)
2300	47.5	7.46	-28.37	16.87	53.60
2350	47.5	7.69	-27.72	16.65	55.86
2400	47.5	7.48	-28.59	16.01	53.21

Applications

- Asymmetrical Doherty amplifier within 2.5-2.7GHz,2.3-2.4GHz
- Sub-3GHz S bandpower amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 2: Pin Connection definition

Transparent top view (Backside grounding for source)

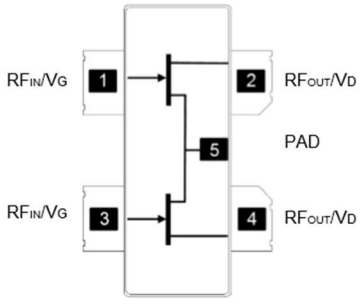


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	46.8	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=50W, on Doherty application board	$R_{\theta JC}$	1.9	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=17mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 17mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=500mA, Measured in Functional Test	$V_{GS(Q)}$		-3.0		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=30mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 30mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=130mA, Measured in Functional Test	$V_{GS(Q)}$		-3.4		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.6GHz, Pout=55W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

2.5-2.7GHz

Figure 3: Efficiency and power gain as function of Pout

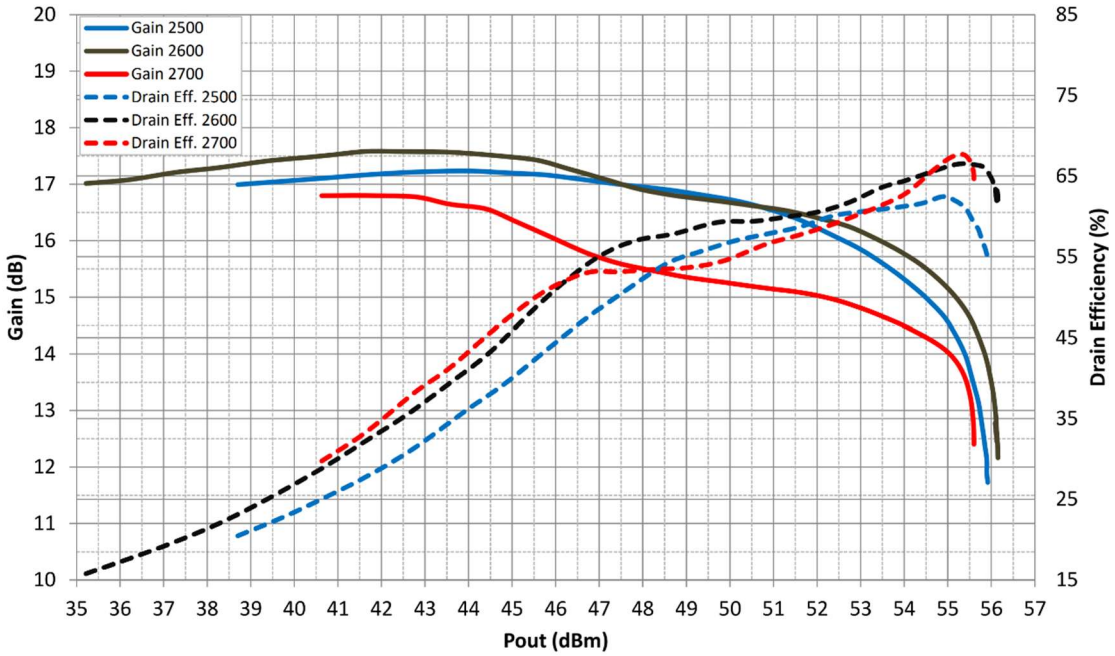


Figure 4: Network analyzer output, S11 and S21

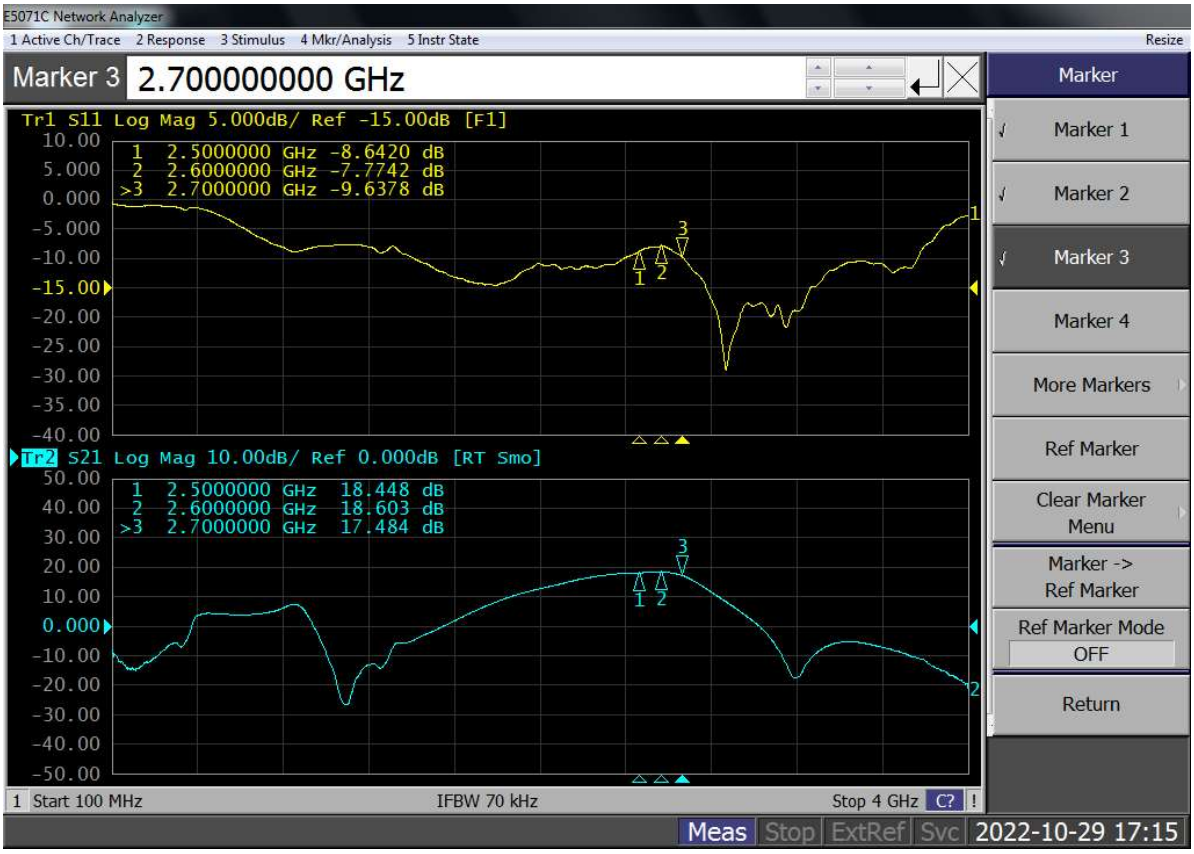


Figure 5: Picture of application board Doherty circuit

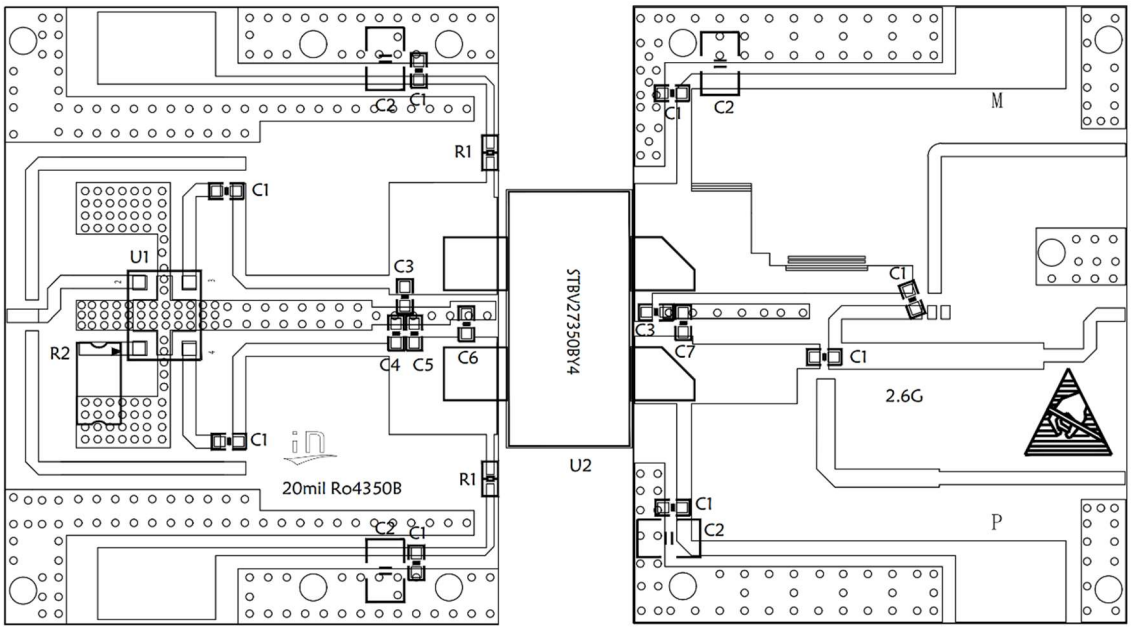


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1	0805	10pF/250V	8
C2	1210	10uF/100V	4
C3	0805	1.0pF/250V	1
C4	0805	0.5pF/250V	1
C5	0805	1pF/250V	1
C6	0805	1.5pF/250V	1
C7	0805	0.6pF/250V	1
R1	0603	10R	2
R2	2512	51R	1
U1	6.35*5.08mm	X3C26P1-03S	1
U2	BY4	STBV27350BY4	1

2.3-2.4GHz

Figure 6: Efficiency and power gain as function of Pout

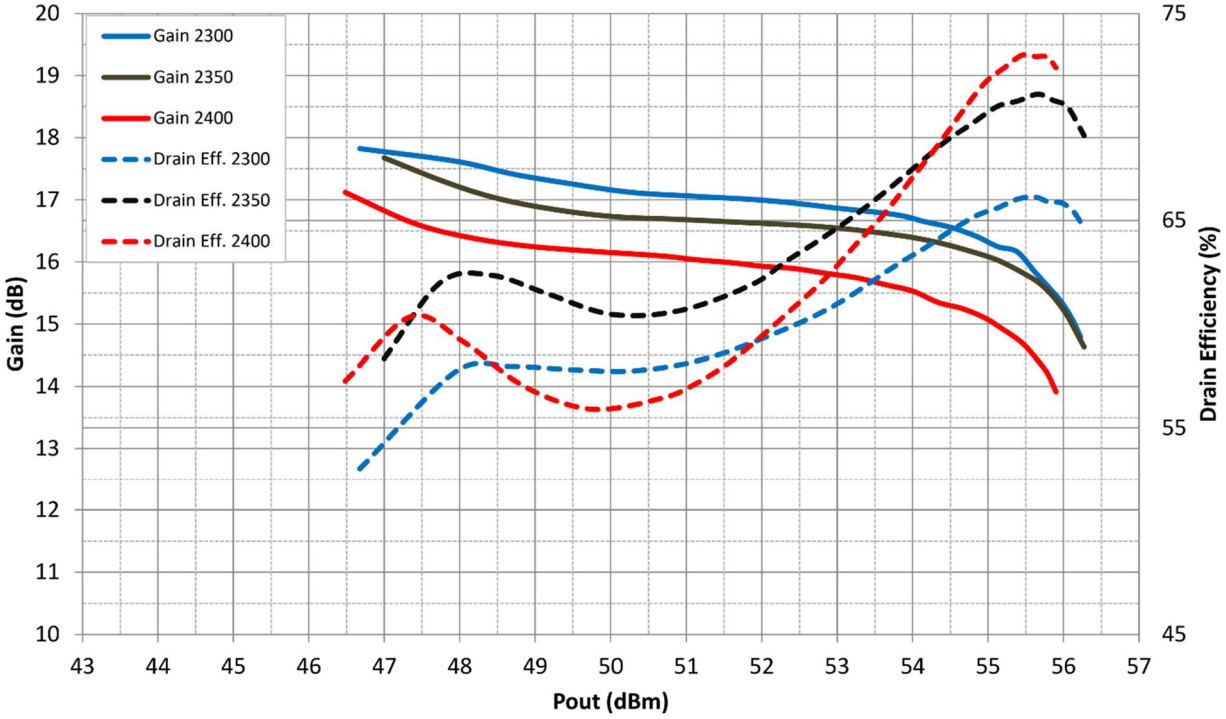


Figure 7: Network analyzer output, S11 and S21

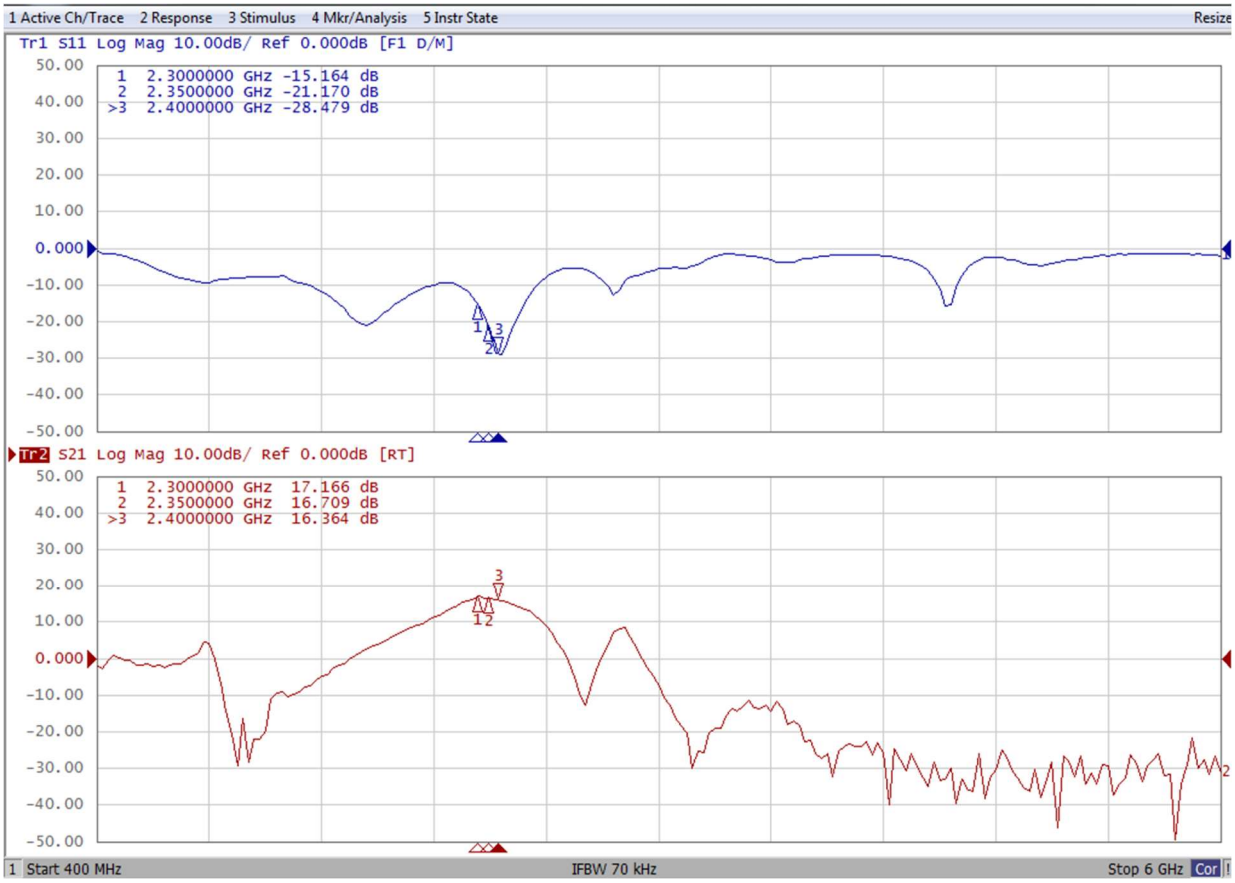


Figure 8: Picture of application board Doherty circuit for 2.3-2.4GHz

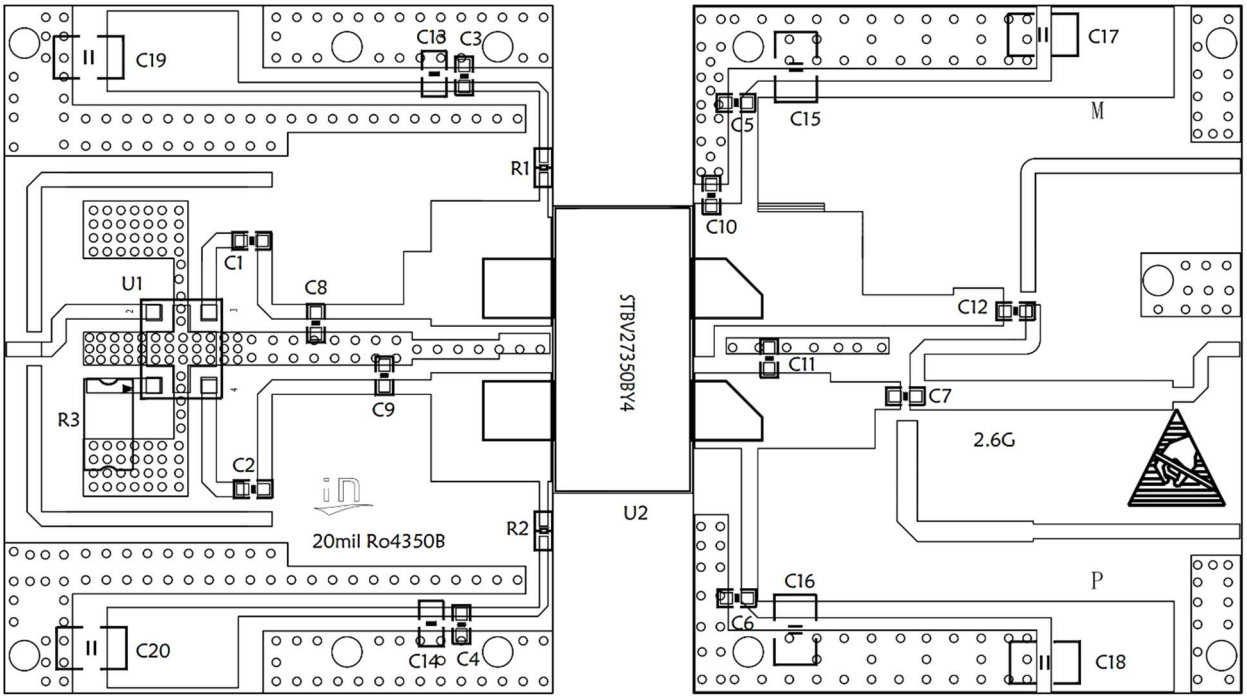
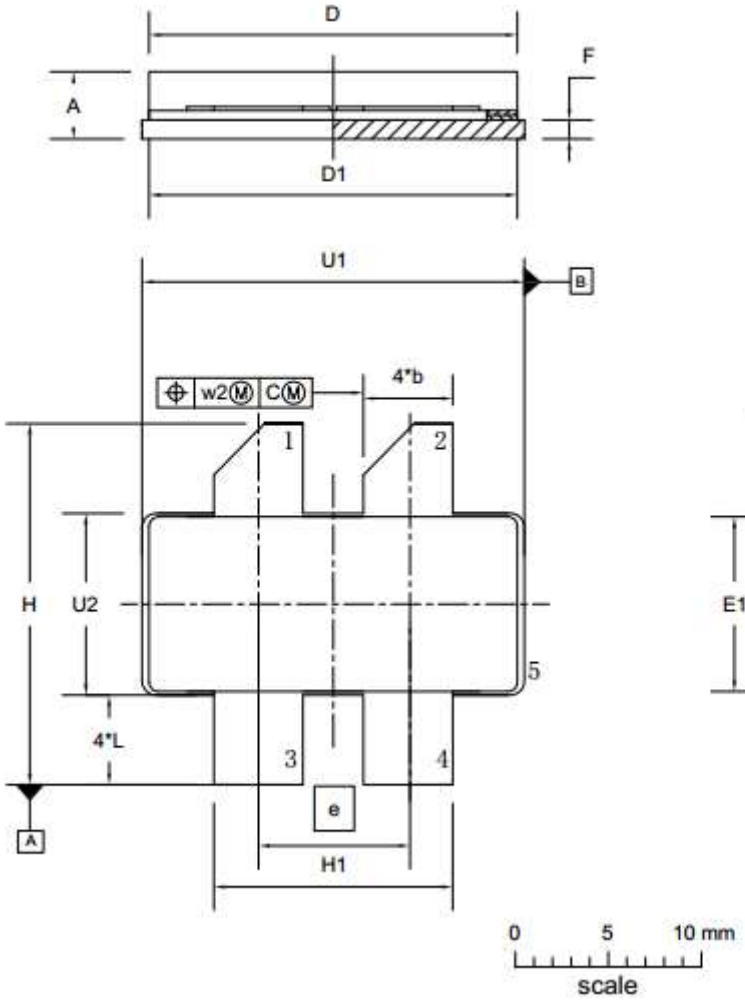


Table 5. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C5, C6, C7	0805	10pF/250V	7
C8	0805	1.0pF/250V	1
C9	0805	0.8pF/250V	1
C10, C11	0805	1.6pF/250V	2
C12	0805	8.2pF/250V	1
C13, C14	0805	10uF/16V	2
C15, C16, C17, C18, C19, C20	1210	10uF/100V	6
R1, R2	0603	10R	2
R2	2512	51R	1
U1	6.35*5.08mm	XC2500P03	1
U2	BY4	STBV27350BY4	1

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2021/12/15	V1.0	Preliminary Datasheet Creation
2022/3/24	V2.0	Device version fixed at V6
2022/10/21	V3.0	Device version updated to V10
2022/11/28	V3.1	Add application data of narrowed band within 2.62-2.69GHz at 45dBm
2024/1/26	V3.2	Add 2.3-2.4GHz application data and remove 2.62-2.69GHz data

Application data based on: ZBB-22-12/15,24-03

Notice