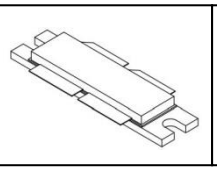
1GHz, 700W, 40V High Power RF LDMOS FETs

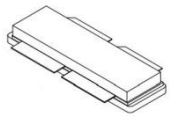
Description

The ITDE10700D4 is a 700-watt, internally matched LDMOS FETs, designed for Multiple ISM and RF Energy applications with frequencies up to 1GHz. It can be used in Class AB/B and Class C for both CW and pulse applications in narrowband operation

ITDE10700D4

ITDE10700D4E





•Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 40 Volts, I_{DQ} = 100 mA, Tcase=25 degree C

Frequency	Signal	Gp (dB)	P_{out}(W)	η_D (%)
915MHz	CW	15	700	68.4
915MHz	100us,10%, Pulsed	15.5	720	69
650MHz	CW	16.5	750	73

Recommended driver: MU1503V operated at 40V

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Optimized for Doherty Applications
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+42	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.16	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	95	——	——	V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 40 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 40V, I_D = 600 uA)	$V_{GS(th)}$	——	2.0	——	V
Gate Quiescent Voltage (V_{DD} = 40 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.6	3.1	V
Functional Tests (On Innogration Test Fixture, 50 ohm system) : V_{DD} =40 Vdc, I_{DQ} = 100 mA, f = 915 MHz, CW Signal Measurements.					
Power Gain	Gp	——	15	——	dB
Drain Efficiency @ P_{SAT}dB	η_D	——	68.4	——	%
Saturated Power	P_{SAT}	——	700	——	W
Input Return Loss	IRL	——	-7	——	dB
Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 40 Vdc, I_{DQ} = 100 mA, f = 915 MHz					
VSWR 10:1 at 700W Output Power at all Phase Angles, pulsed CW, 100us, 10%	No Device Degradation				

Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request)

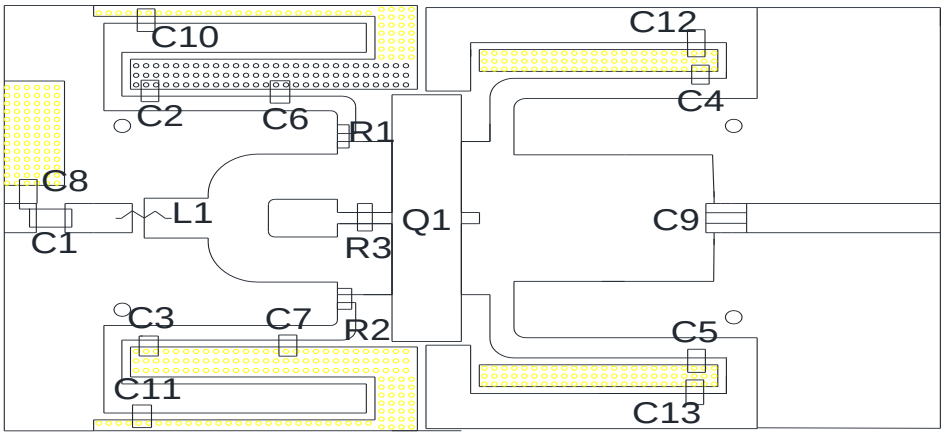


Figure 1. 915MHz Test Circuit Component Layout

Table 5. 915MHz Test Circuit Component Designations and Values

Component	Description	Specification
C1~C5	56PF	ATC800B
C6,C7	47PF	ATC800B
C8	1PF	ATC800B
C9	18PF*3	ATC800B
C10,C11	10UF	1210
C12,C13	Electrolytic Capacitor ,1000UF	50V/1000UF
L1	0.5 turns	Φ1mm varnished wire
R1,R2,R3	10Ω	1206
Q1	ITDE10750D4	
PCB	Taconic RF-60TC	25Mil

TYPICAL CHARACTERISTICS

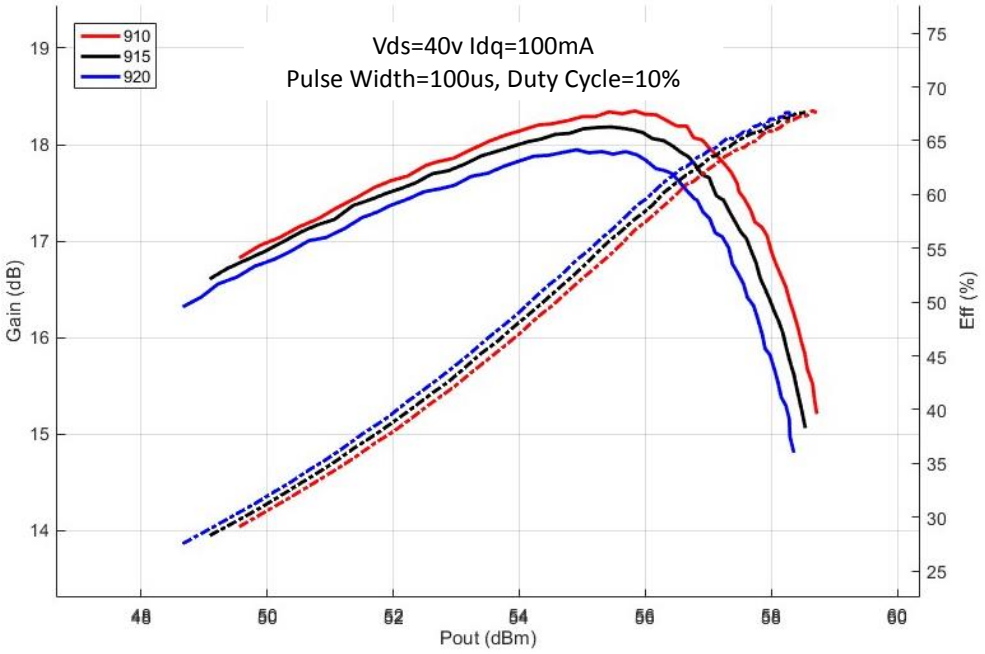
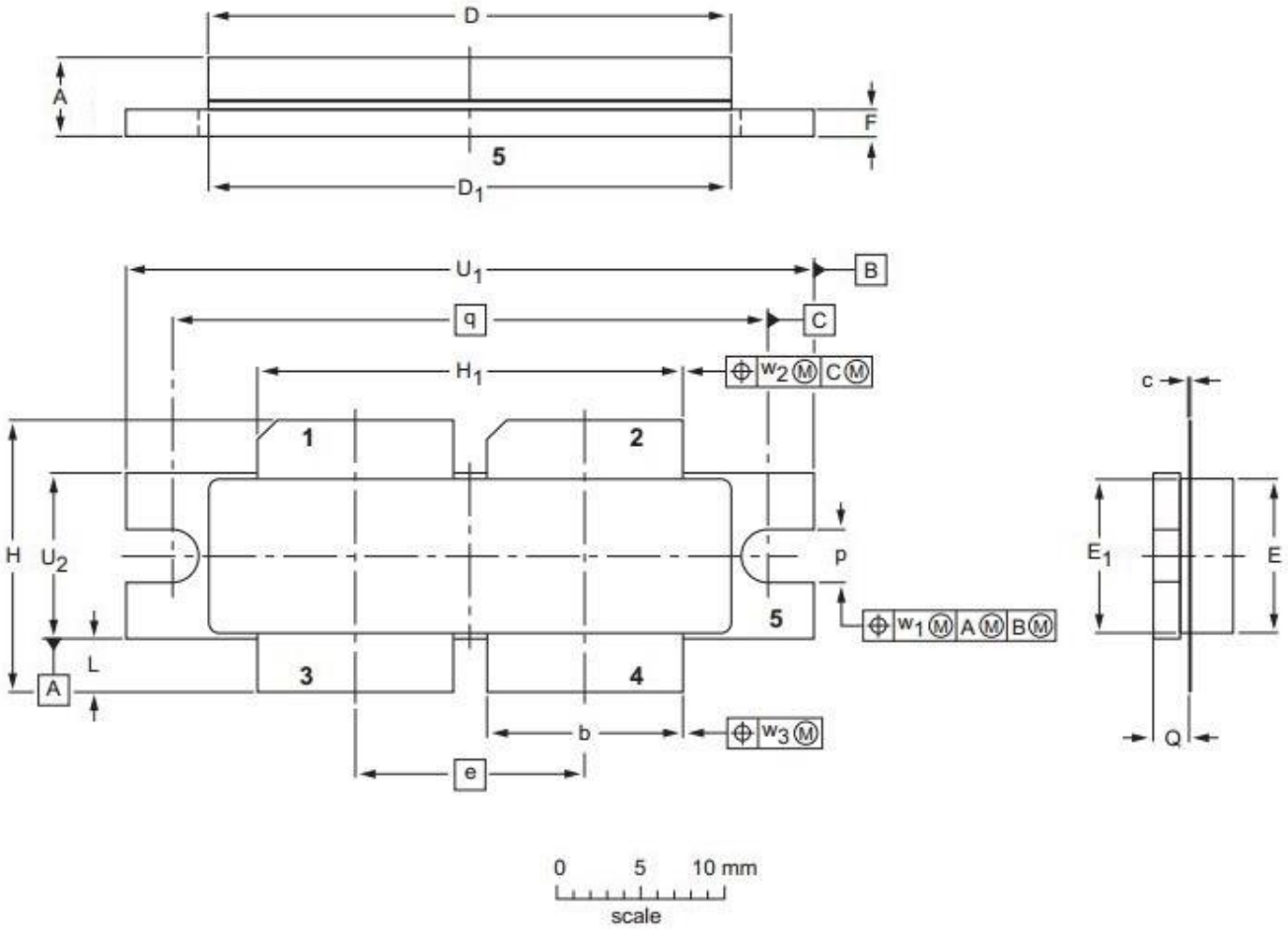


Figure 2. Drain Efficiency and Power Gain as Function of Pulse CW Output Power

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

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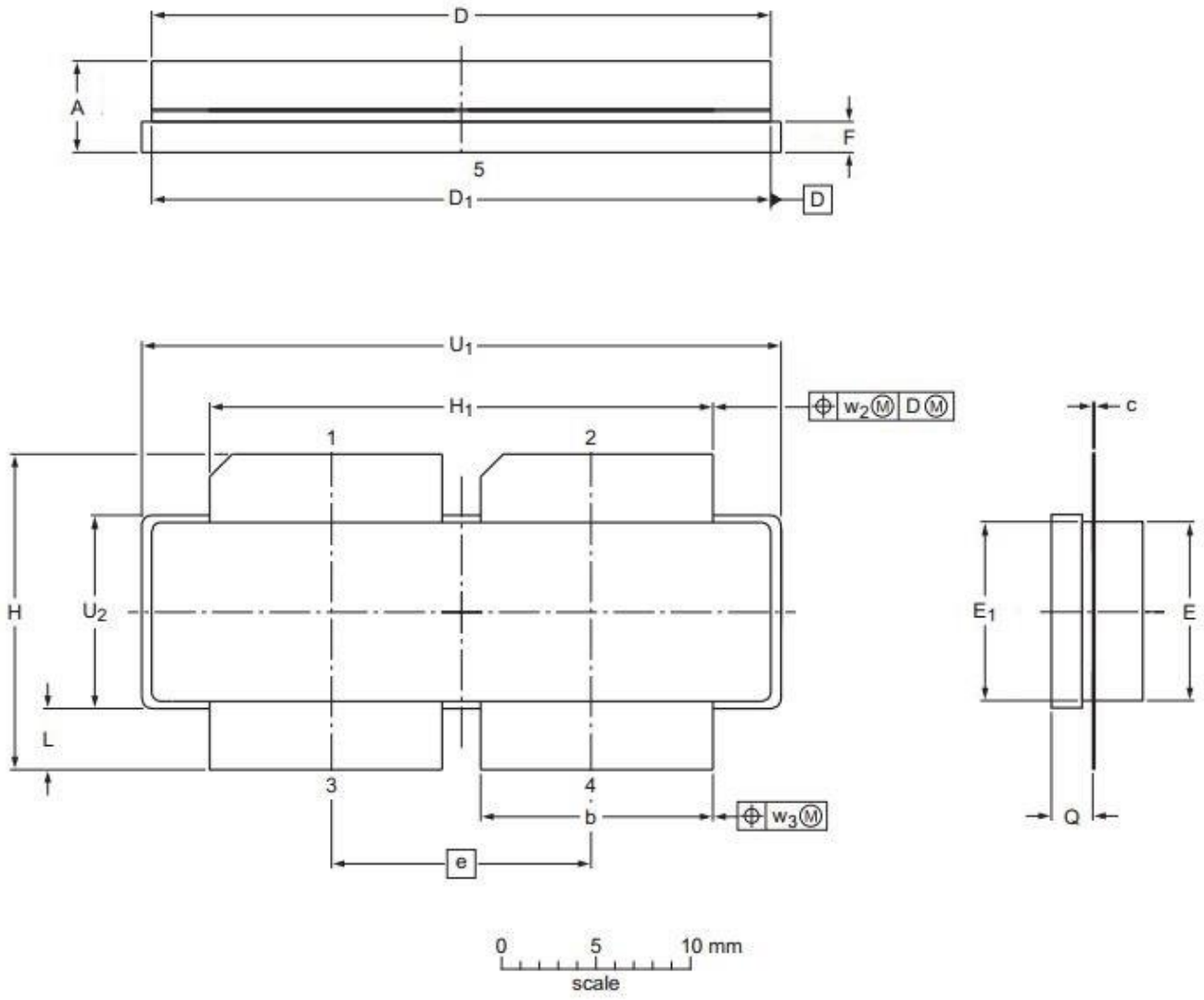
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Earless flanged ceramic package; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	Q	U_1	U_2	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	2.26 2.01	32.39 32.13	10.29 10.03	0.25	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.089 0.079	1.275 1.265	0.405 0.395	0.01	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2018/07/19	Rev 1.0	Preliminary Datasheet
2018/07/26	Rev 1.1	Add VSWR info
2018/08/10	Rev 1.2	Add 650MHz application result

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