M2M20R5V LDMOS TRANSISTOR

Document Number: M2M20R5V
Production Datasheet V1.0

2GHz, 5W, 50V High Power RF LDMOS FETs

M2M20R5V

Description

The M2M20R5V is a 5-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 2GHz.

It can support pulsed, CW or any modulated signal in form of linear or saturated operations.

- Typical Performance (On Innogration narrow band fixture with device soldered):

Pulsed CW, 20uS width，10% dule cycle

V_{DS}= 50V，I_{DQ}=3mA，V_{GS} =3.17V

FREQ (MHZ)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2000	36.9	4.89	51.91	16.93	37.8	6	55

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 30-512MHz (Jammer, Ground/Air communication)
- 4G/5G cellular base station
- 470-860MHz (TV UHF)
- Avionics 960-1215MHz
- L band 1200-1400MHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		115		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.73	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 5 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.16	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		5.8		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		2.5		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		0.02		pF
Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 3mA, f = 2GHz, Pulsed CW Signal Measurements, Pin=19dBm					
Power Gain@Pout	G_p	——	18	——	dB
Output Power	Pout		5		W
Drain Efficiency@Pout	η_D	50	55	——	%
Input Return Loss	IRL	——	-5	——	dB

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout at 2GHz

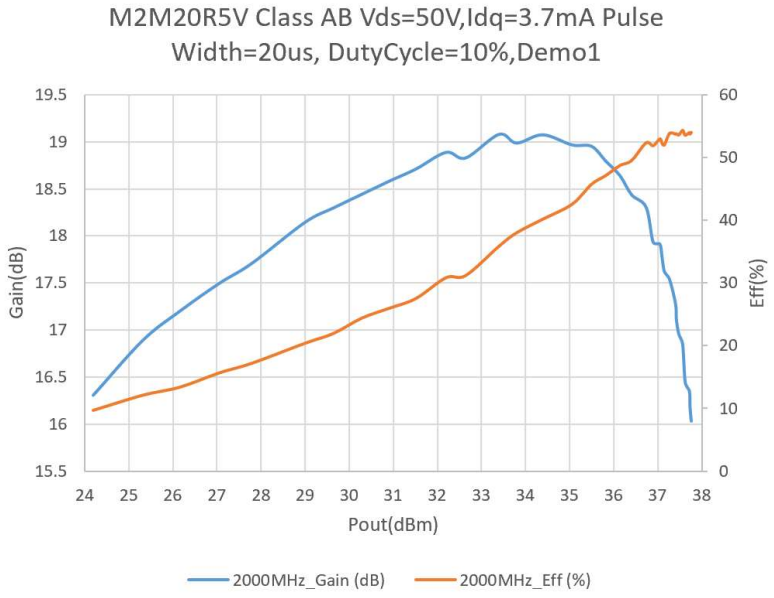


Figure 2: Network analyzer output S11/S21

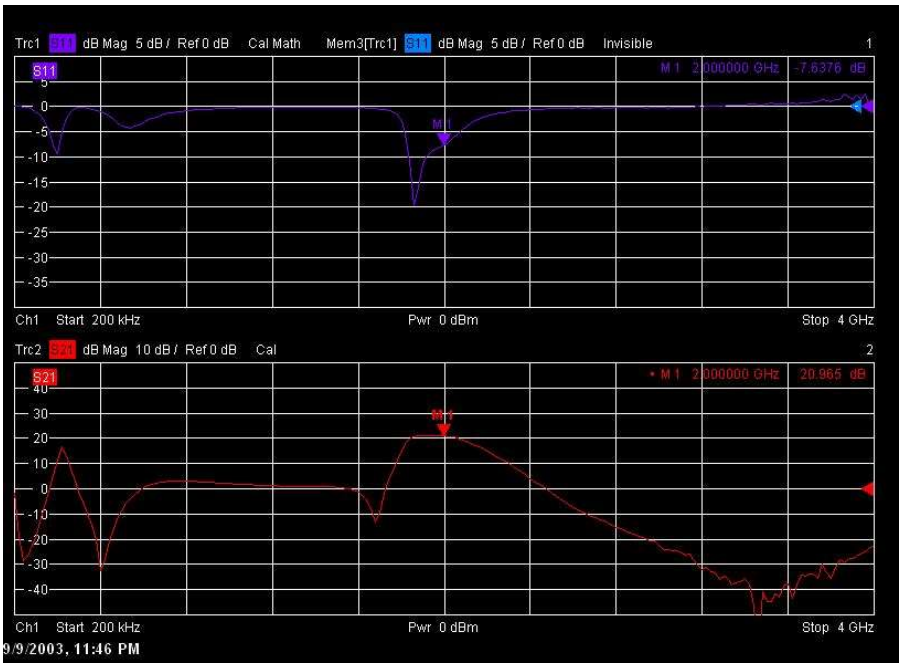
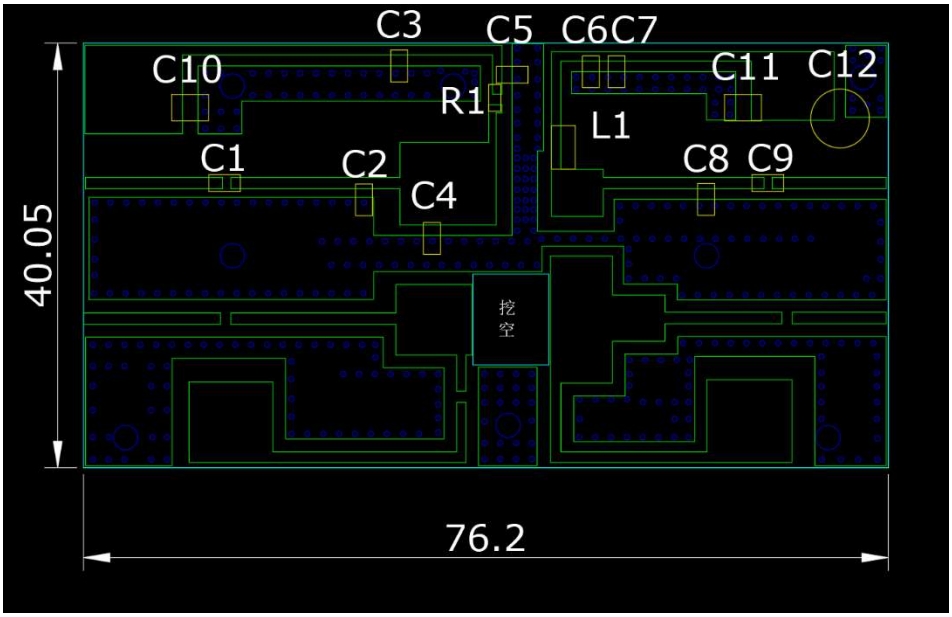


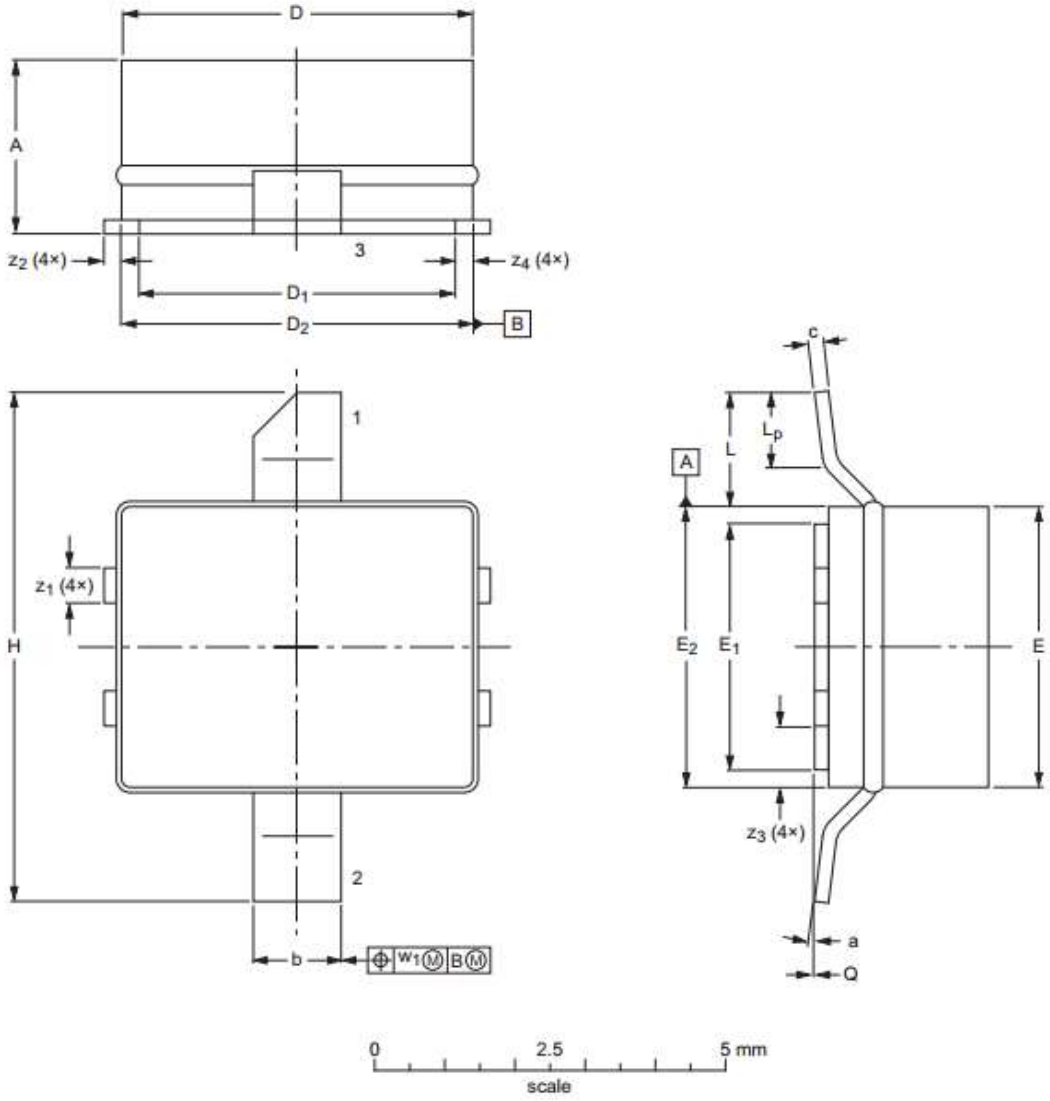
Figure 3. Test Circuit Component Layout (PCB Roger 4350B 20Mil, PCB file upon request)



Component	Value	Quantity
U1	M2M20R5V	1
C1、C6、C7、C8	33pF	4
C3、C4	15pF	2
C2	10pF	1
C5	12pF	1
C11	470uF/63V	1
C9、C10	10uF	2
R1	10Ω	1

Package Outline

Earless Flanged ceramic package; 2 leads(1-Drain,2-Gate,3-Source)



UNIT	A	b	c	D	D_1	E	E_1	E_2	H	L	L_P	Q	w_1	z_1	z_2	z_3	z_4	α
mm	2.34	1.35	0.23	5.16	4.65	4.14	3.63	4.14	7.49	2.03	1.02	0.1	0.25	0.58	0.25	0.97	0.51	7°
	2.13	1.19	0.18	5.00	4.50	3.99	3.48	3.99	7.24	1.27	0.51	0.0		0.43	0.18	0.81	0.00	0°

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-MM					18/6/2014

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/12/15	**V1.0**	**Production Datasheet Creation**

Application data based on ZYX-22-12

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