



20W,28V Plastic RF LDMOS Transistor

ITEH38020C6

Description

The ITEH38020C6 is a 20-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies 3.3 to 3.8GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It is part of low power general purpose plastic LDMOS with pin to pin compatibility.

• Typical 3.3-3.6GHz Class AB RF Performance (On Innogrator fixture with device soldered).

VDS=28V, IDQ=160mA, Vgs=2.69V



FREQ (MHZ)	POUT (DBM)	CCDF (DB)	ACPR (DBC)	GAIN (DB)	EFFICIENCY (%)
3300	32.01	9.93	-47.9	14.2	13.1
3450	32.01	10.00	-47.7	14.4	14.1
3600	32.00	9.76	-47.4	13.7	14.6

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- S band power amplifier
- All 4G/5G cellular application within 3.3 to 3.8GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+28	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j =200°C, DC test	R _{θJC}	0.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2



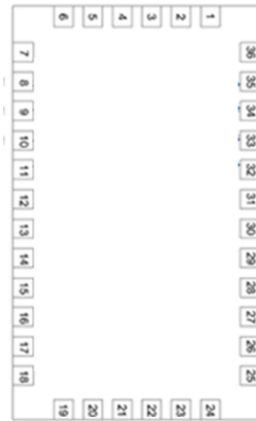
Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V _{GS} =0, I _{DS} =100uA	V _{(BR)DSS}		65		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate--Source Leakage Current (V _{GS} = 11 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 600 μA)	V _{GS(th)}	—	2	—	V
Gate Quiescent Voltage (V _{DD} = 28V, I _D = 160mA, Measured in Functional Test)	V _{GS(Q)}	—	2.7	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 100 mA, f = 3600 MHz

VSWR 10:1 at 20W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Definition(Top View)



Pin No.	Symbol	Description
8,9,10,11	Vgs/RF In	Vgs and RF input
32,33,34,35	Vds/RF out	Vds and RF output
2,5,7,12,13,18,20,23,25,30,31,36	GND	DC/RF Ground
Others	NC	No connection
Package Base	GND	DC/RF Ground.

Reference Circuit of Test Fixture Assembly Diagram
3300-3600MHz RO4350B 20mils

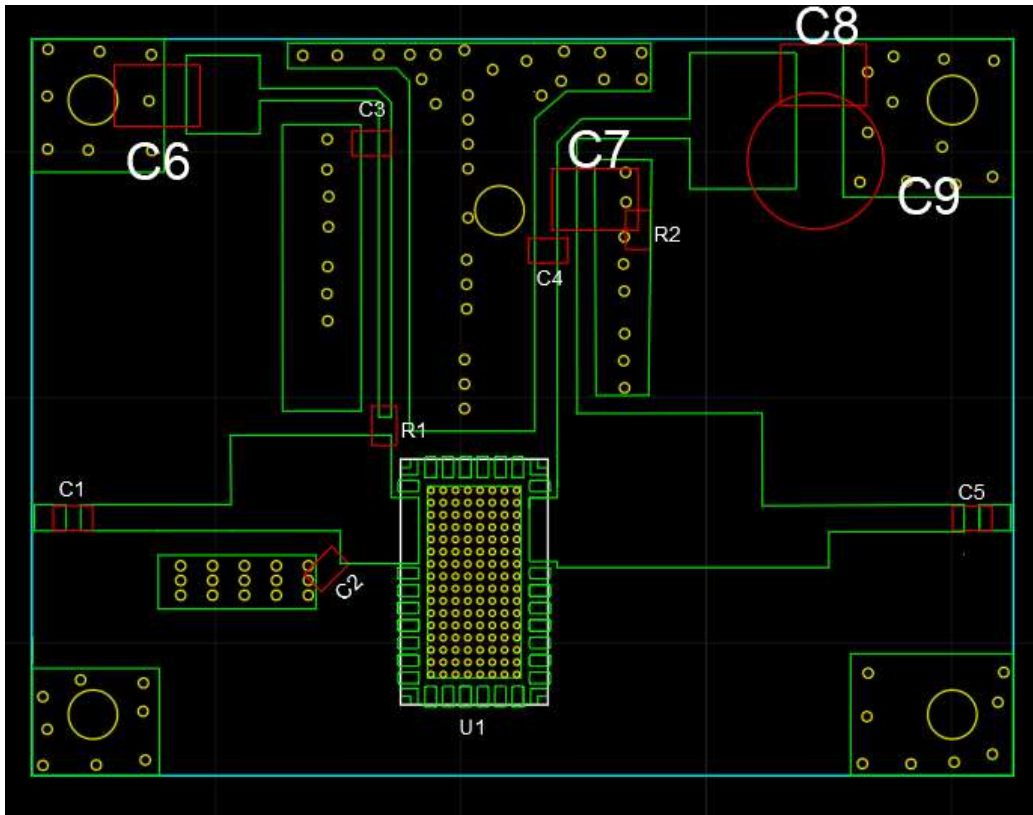


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
U1	ITEH38020C6	1
C1、C5	8.2pF	2
C3、C4	12pF	2
C6、C7、C8	10uF/63V	3
R1、R2	10 Ω	2
C9	470uF/63V	1
C2	1.2pF	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Out

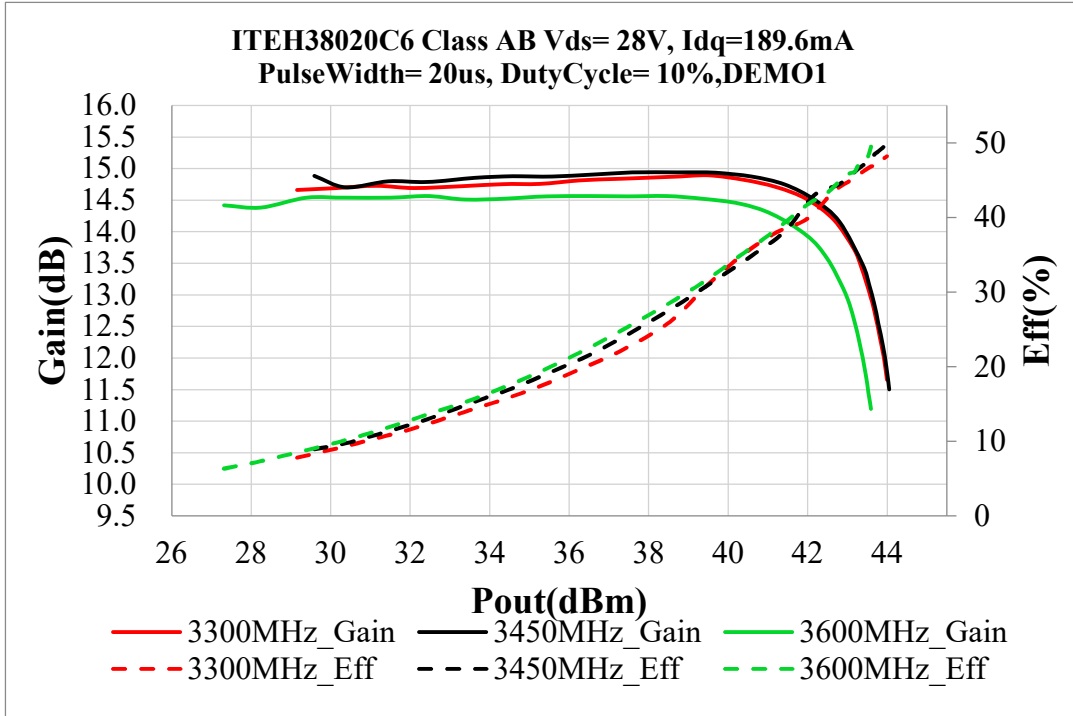
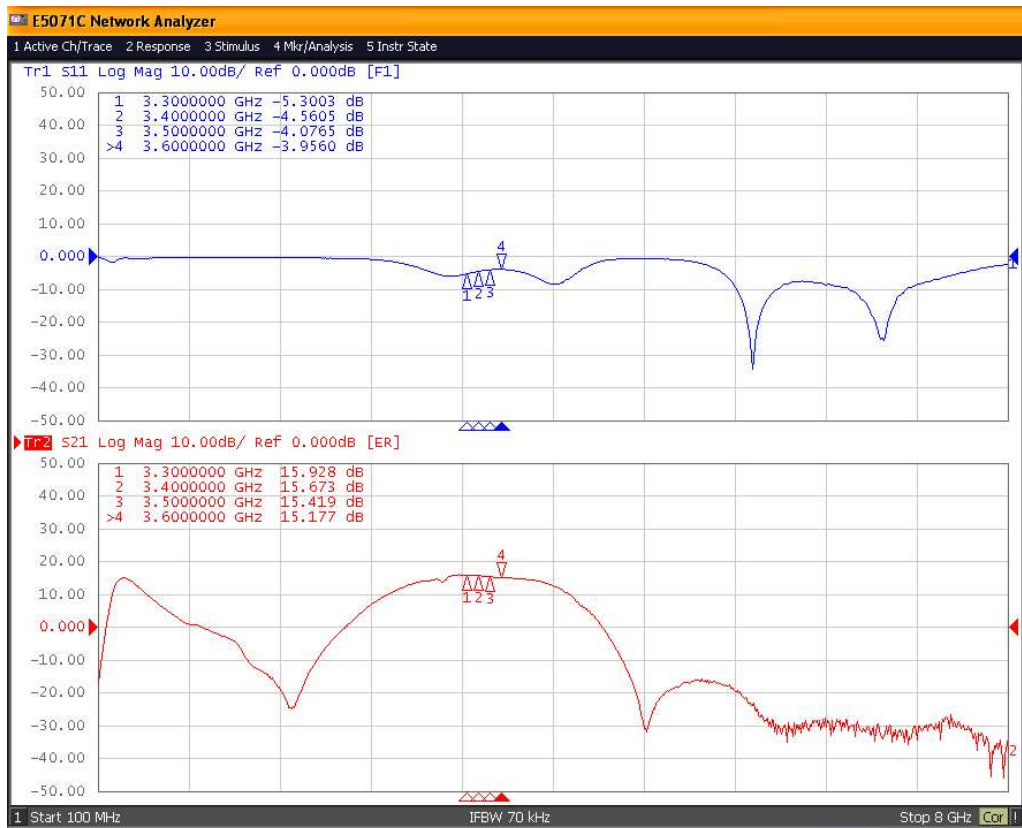


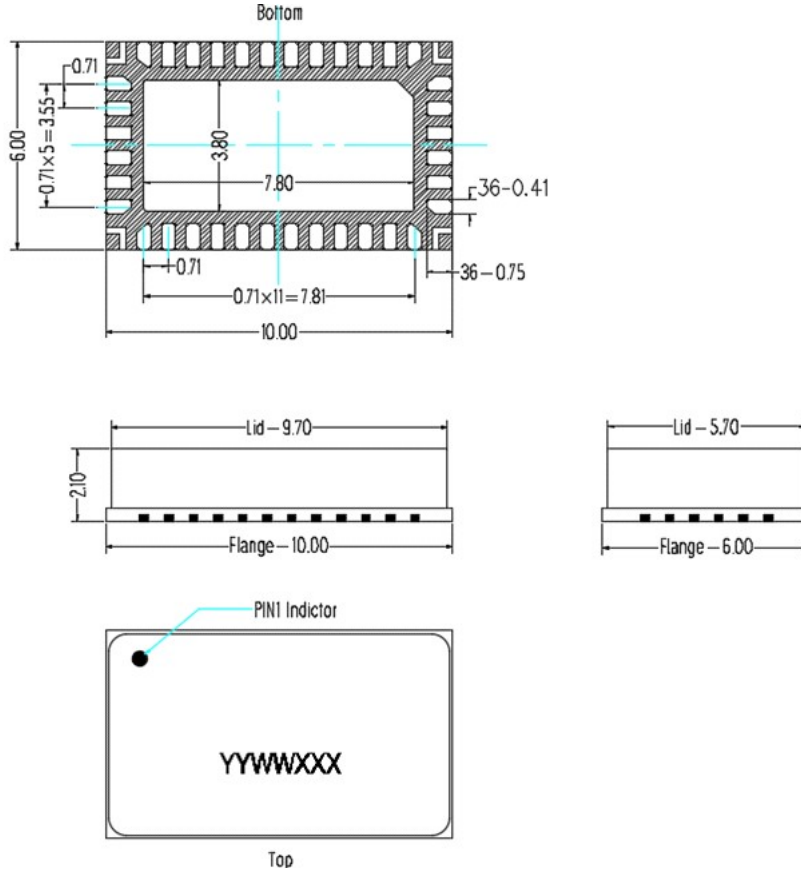
Figure 4. Network analyzer output S11/S21





Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2022/10/19	Rev 1.0	Preliminary Datasheet
2022/12/9	Rev 1.1	Update on Pin Definition

Application data based on ZXY-22-10

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