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Gallium Nitride 50V, 130W, 0.1-3.8GHz RF Power Transistor

Description

The STBV38130E2 is a 130watt, GaN HEMT, ideal for general applications from 0.1 to 3.8GHz. It can support CW, pulse or any modulated signal.

It features high gain, wide band and low cost, in 6.5*6.5mm ceramic package with copper flange. Its gullwing leads enable surface mounted on PCB through grounding vias or soldered on heatsink There is no guarantee of performance when this part is used outside of stated frequencies.

• Typical Class AB performance 3.4-3.8GHz: (On application board with device soldered)

VDD = 50 Vdc, IDQ = 150 mA,1 Carrier WCDMA signal

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Freq	Pout	CCDF	Ppeak	Ppeak	ACPR	Gain	Efficiency
(MHz)	(dBm)	(dB)	(dBm)	(W)	(dBc)	(dB)	(%)
3400	43.14	8.87	52.01	158.8	-39.3	13.2	24.3
3500	43.16	8.73	51.89	154.5	-38.6	13.6	25.3
3600	43.17	8.55	51.72	148.6	-37.5	13.7	26.3
3700	43.15	8.45	51.60	144.6	-36.6	13.7	27.2
3800	43.17	8.22	51.39	137.8	-35.9	13.1	27.3

Applications

- 5G, 4G wireless infrastructure
- S band power amplifier
- Test instruments
- Jammer

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

- 1. Set VGS to the pinch--off (VP) voltage, typically -5 V
- 2. Turn on VDS to nominal supply voltage
- 3. Increase VGS until IDS current is attained
- 4. Apply RF input power to desired level

Turning the device OFF

- 1. Turn RF power off
- 2. Reduce VGS down to VP, typically -5 V
- 3. Reduce VDS down to 0 V
- 4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit		
DrainSource Voltage	V _{DSS}	+200	Vdc		
GateSource Voltage	V_{GS}	-8 to +0.5	Vdc		
Operating Voltage	V_{DD}	55	Vdc		
Maximum gate current	lgs	16.8	mA		
Storage Temperature Range	Tstg	-65 to +150	°C		
Case Operating Temperature	T _C	+150	°C		
Operating Junction Temperature	TJ	+225	°C		

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA	Do 10	2.2	°C /W
T _C = 85°C, at Pavg=25W WCDMA 1 carrier	R⊕JC	2.2	-C /VV



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Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=16.8mA	V _{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 16.8mA	$V_{GS(th)}$	-4	-3	-2	V
Gate Quiescent Voltage	iescent Voltage VDS =50V, IDS=150mA, Measured in Functional Test			-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit
Load mismatch capability	3.6GHz, Pout=130W pulse CW					
	All phase,	VSWR		10:1		
	No device damages					

Figure 1: Efficiency and power gain as function of Pout (Measured on 3.4-3.8GHz application board)

VDD = 50 Vdc, IDQ = 150 mA, Pulse width=20us, duty cycle=20%

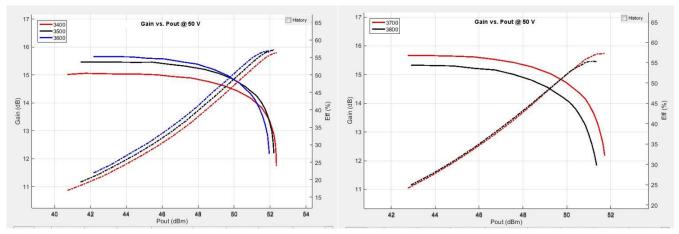


Figure 2: Network plot for S11/S21

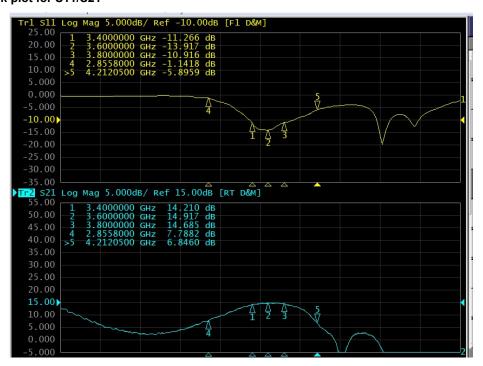


Figure 3: Picture of application board of 3.4-3.8GHz

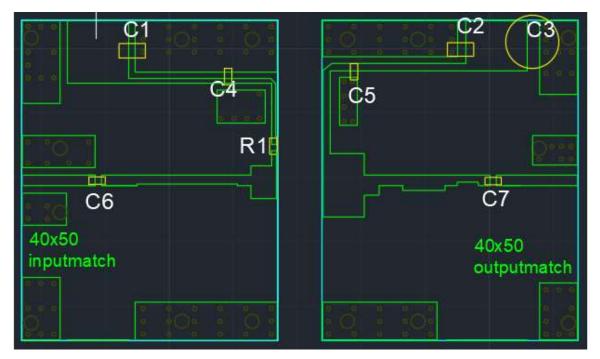


Table 4. Bill of materials of application board, RO4350B 30Mils (PCB layout upon request)

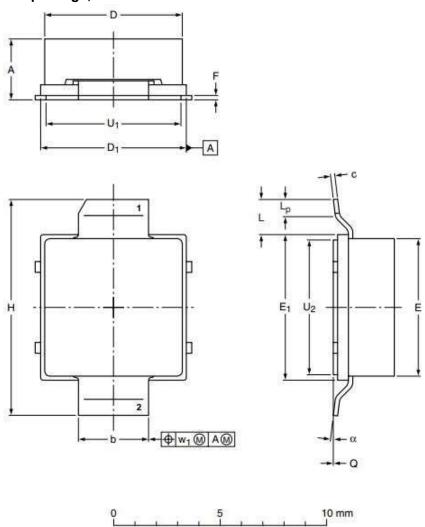
Designator	Comment	Footprint	Quantity
C1, C2	10uF/100V	1210	2
C3	470uF/63V		1
C4, C5, C6, C7	8.2 pF	0603	4
R1	10ohm	0603	1



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Package Outline

Earless Flanged ceramic package; 2 leads



UNIT	А	b	С	D	D ₁	E	E ₁	F	н	L	L _P	Q	Uı	U ₂	W ₁	α
	3.63	3.38	0.23	6.55	6.93	6.55	6.93	0.23	10.29	1.65	1.02	+0.05	6.43	6.43	0.51	7°
mm	3.05	3.23	0.18	6.40	6.78	6.40	6.78	0.18	10.03	1.65	0.51	-0.05	6.27	6.27	0.51	0°
inahaa	0.143	0.133	0.009	0.258	0.273	0.258	0.273	0.009	0.405	0.005	0.040	+0.002	0.253	0.253	0.00	7°
inches	0.120	0.127	0.007	0.252	0.267	0.252	0.267	0.007	0.395	0.065	0.020	-0.002	0.247	0.247	0.02	0°

OUTLINE		REFER	RENCE	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	1330E DATE
PKG-E-A						10/22/2013



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Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2021/11/25	V1.0	Preliminary Datasheet Creation
2022/2/28	V1.1	Modification of frequency lower limits to 0.1GHz

Application data based on: ZXY-21

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