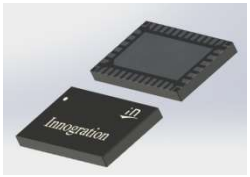
2.5-2.7GHz, 60W, 50V GaN Doherty PA Module

Description



The SMAV2527-60 is a 60-watt, integrated 2-stage Power Amplifier Module, designed for 5G massive MIMO applications, with frequencies from 2.5 to 2.7GHz. The module is 50 Ω input fully matched and output partially matched, and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions，with much less sensitivity for production, housed in 10*6mm cost effective plastic open cavity package, and heat dissipated by copper flange.

The module incorporates advanced Doherty circuit delivering high power added efficiency for the entire module at 11 W average power according to normal 8 dB back off.

Innogration owns the patents for internal Doherty architecture, and related plastic open cavity.

•Typical Performance of Doherty Demo (On Innogration fixture with device soldered through grounding vias):
VDS= **46**V, IDQ-main=70mA Vgs-main=-2.8V. Vgs-peak=-4.8V, Idq-driver=18mA, Vgs-Driver=-3.0V

Freq (GHz)	Pulse CW Signal(1)			Pavg=39.5dBm WCDMA Signal(2)		
	P1-Gain (dB)	P3 (dBm)	P3 (W)	Gp (dB)	Eff(%)	ACPR5M (dBc)
2.5	30.8	47.6	57.5	30	50	-30
2.6	31.9	47.8	60.2	30.9	50.5	-28
2.7	32	47.6	57.5	30.8	50	-28

Notes:
(1) Pulse Width=100 us, Duty cycle=20%
(2) WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz,PAR =10.5 dB at 0.01 % probability on CCDF.

Features and Benefits

- Adjustable drain bias to fit different power demand
- Extremely good VBW performance to enable the broadest IBW/OBW
- Industry leading RF performance for 5G MIMO AAU, for instance
  - ✓ 64T:320W
  - ✓ 32T:160W
- Plastic open cavity without molding compound brings advantage compared to molded design
  - ✓ Minimize the risk of high density thermal distribution in fanless system for longer life time
  - ✓ Highly consistent RF performance for yield of volume production
- 50 Ω Input matched, output partially matched, effective PCB space smaller than 12*20mm
- Integrated Doherty Final and driver Stage
- 6x10 mm Surface Mount Package, full copper flange underneath for grounding and heat dissipation, much more effective than LGA PCB based design

Pin Configuration and Description

Pin No.	Symbol	Description
6	RF IN	RF Input
1	VDS-driver	Driver stage, Drain Bias
4	VGS-driver	Driver stage, Gate Bias
19,21	RF Out2	RF Output，Drain Bias of Main Amplifier
22,24	RF Out1	RF Output, Drain Bias of Peaking Amplifier
11	VGS-main	Main Amplifier, Gate Bias
32	VGS-peak	Peaking Amplifier, Gate Bias
3,8-10,14,15,16,17,26,27,28,29,33-35	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36	GND	Internal Grounding, recommend connecting to Epad ground
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.6	Vdc
Operating Voltage	V_{DD}	+60	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance@Average Power, Junction to Case Tcase=+85℃，CW Test，，Pout=8W,	RθJC	6.5	°C/W

Notes:
(1) The thermal resistance is acquired by our company's FEA model,which was calibrated by IR measurement,the value shall be applied to reliability.
(2) The reference Tcase temperature 85℃ is apply on the backside of package.
(3) If the device soldering onto the 20mil Rogers PCB with 108×Φ0.25mm via hole beneath the package backside and the reference temperature Tcase（85℃） apply on the groundside of the PCB, the total thermal resistance Rθ JC (TBD)℃/W.
(4) The power dissipation in the table is overall dissipation which includes Carrier PA, Peaking PA and driver PA.

Table 3. ESD Protection Characteristics

Test Methodology	Class Voltage
Human Body Model(HBM) (JEDEC Standard JESD-A114)	TBD
Charged Device Model (CDM) (JEDEC Standard JESD22-C101F)	±1000V

Table 4. Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		2.5		2.7	GHz
Driver Quiescent Current ($I_{DQ\text{-}driver}$)			18		mA
Carrier Quiescent Current ($I_{DQ\text{-}main}$)			70		mA
Peak PA Gate Quiescent Voltage (V_{PEAK})			-4.8		V
Power Gain @ Pout=39dBm	Freq=2.6GHz		29		dB
Efficiency @Pout=39dBm	Freq=2.6GHz		50		%
Ppeak by CCDF	Freq=2.6GHz	60			W

Load Mismatch of per Section (On Test Fixture, 50 ohm system): f = 2.6GHz

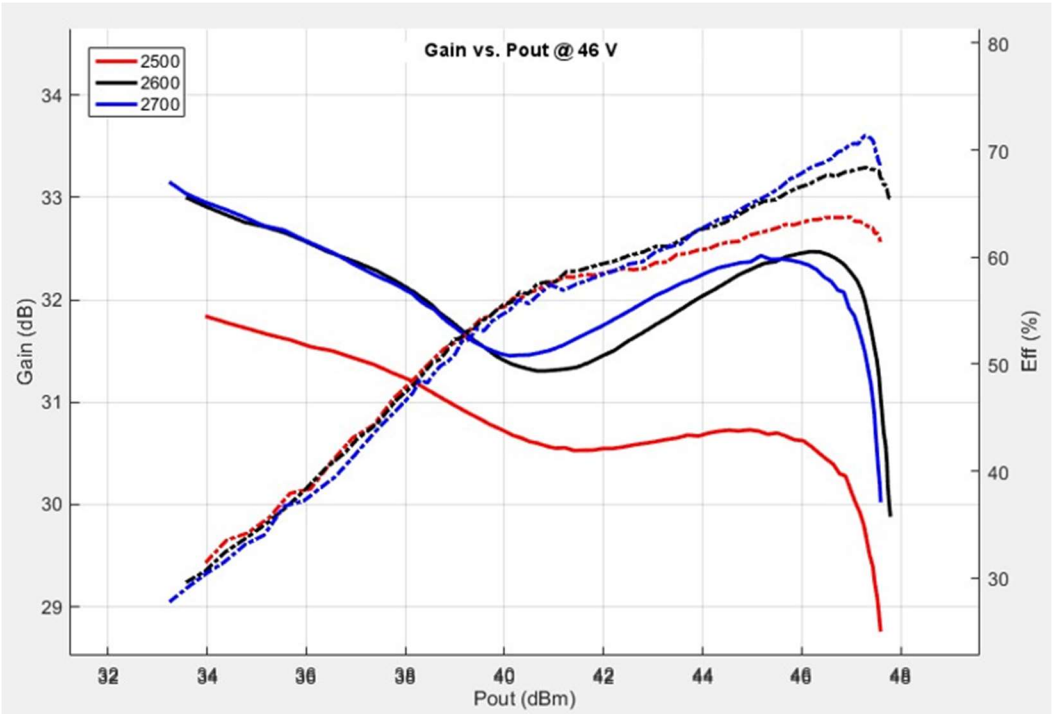
VSWR 10:1 at P3dB pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Application board and its layout info based on request

Figure 1. Power Gain and Drain Efficiency as Function of Pulsed CW Output Power

VDS= **46**V, IDQ-main=70mA Vgs-main=-2.8V. Vgs-peak=-4.8V, Idq-driver=18mA, Vgs-Driver=-3.0V



Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2500	39.53	8.98	54.28	30.83	47.60	57.50	61.36
2600	38.54	7.15	50.10	31.95	47.79	60.17	65.48
2700	38.14	6.52	47.24	32.06	47.60	57.52	68.32

Figure 2. Network analyzer output S11/S21

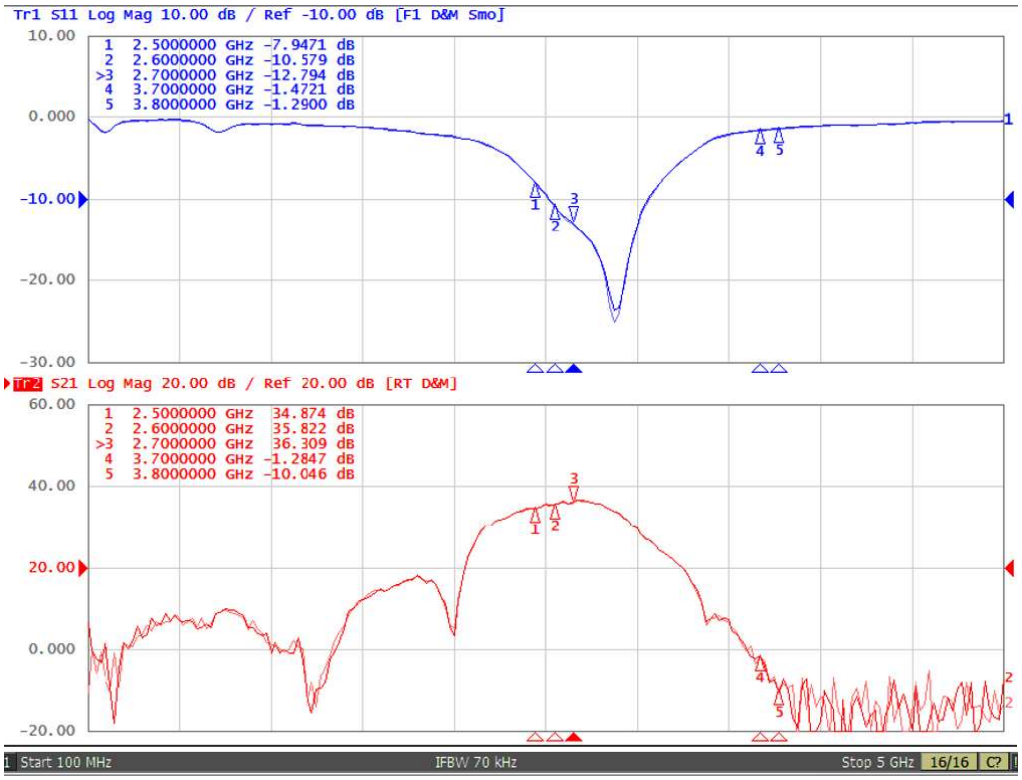


Figure 3. Video Impedance Test

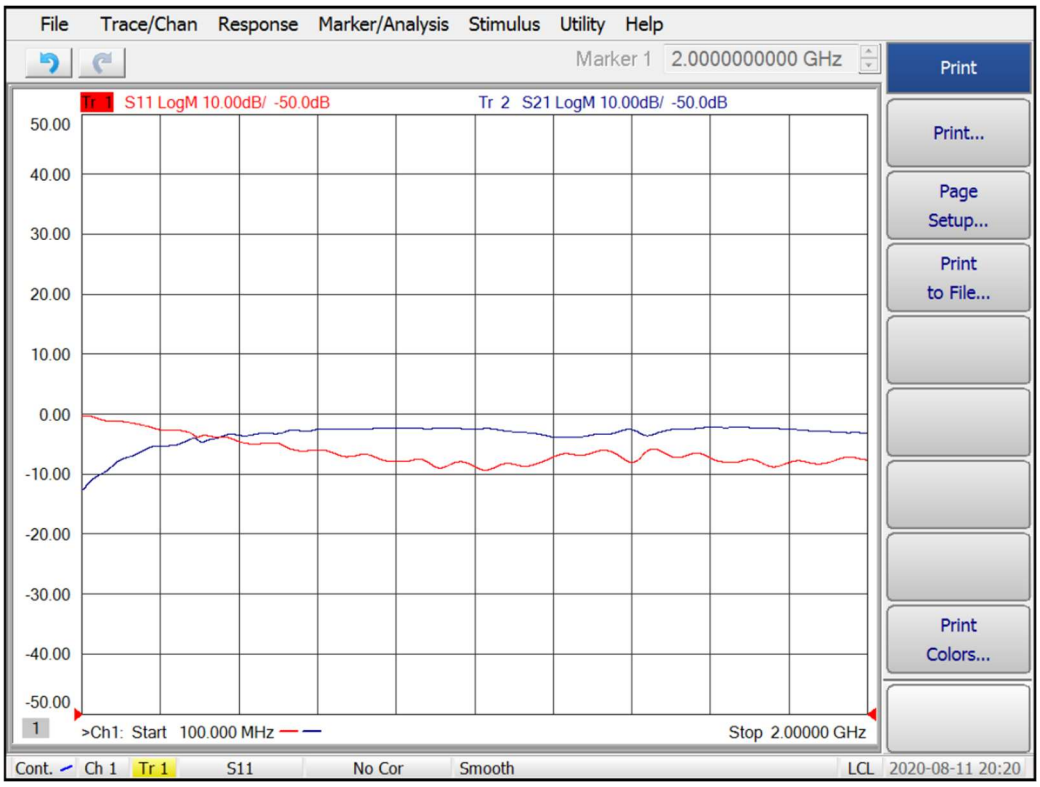
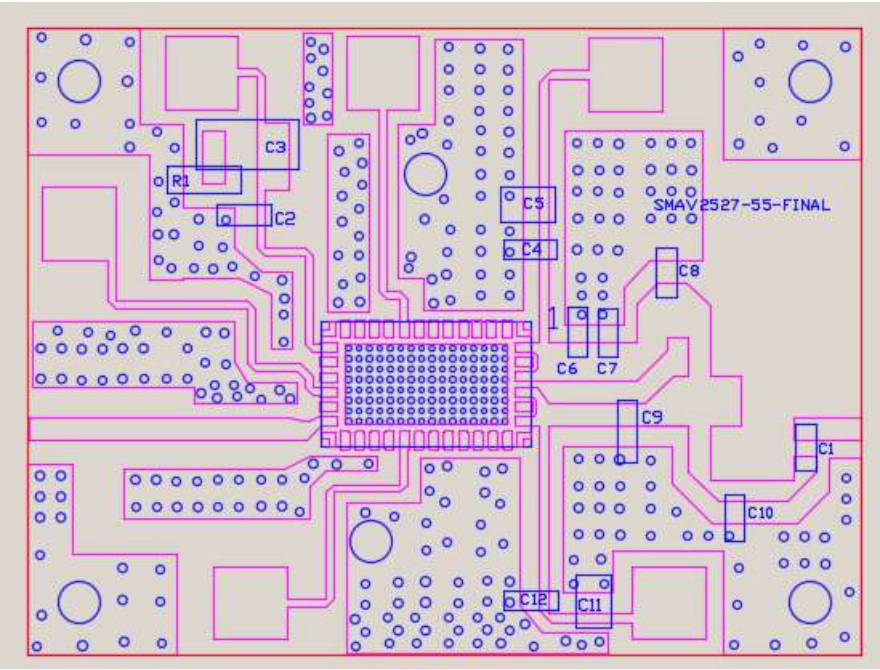


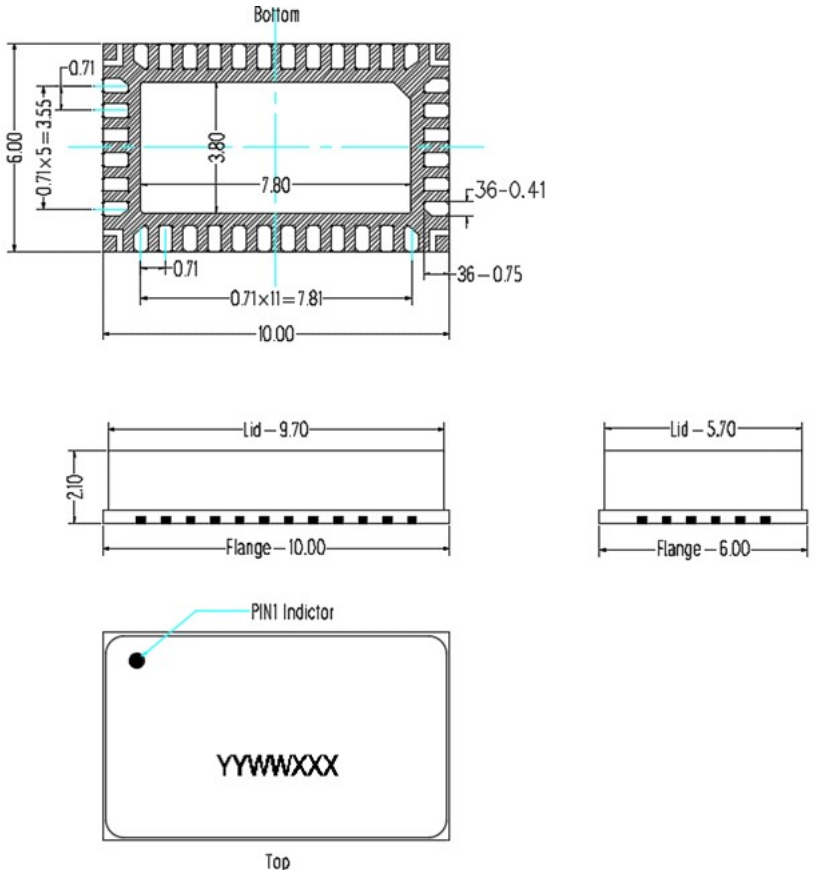
Figure 4. Application board layout info



BOM				
Part	**Quantity**	**Description**	**Part Number**	**Manufacture**
C1,C2,C4,C12	4	10pFHigh Q Capacitor	251SHS100BSE	TEMEX
C6	1	2.0pFHigh Q Capacitor	251SHS2R0BSE	TEMEX
C7	1	0.4pFHigh Q Capacitor	251SHS0R4BSE	TEMEX
C8	1	0.7pFHigh Q Capacitor	251SHS0R7BSE	TEMEX
C3,C5,C11	3	10uF MLCC	RS80R2A106M	MARUWA
C9,C10	2	1.0pFHigh Q Capacitor	251SHS1R0BSE	TEMEX
R1	1	10Ω Power Resistor	ESR03EZPF100	ROHM

Package Dimensions

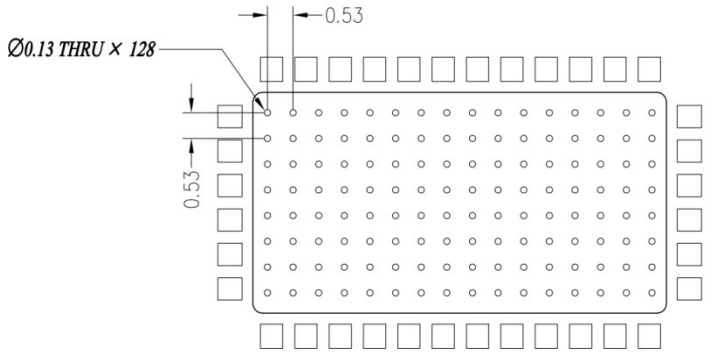
10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/11/24	Rev 1.0	Preliminary Datasheet
2022/3/30	Rev 1.1	Modified pins definition of drain bias for main and peak path

Application data based on LWH-21-12

Disclaimers