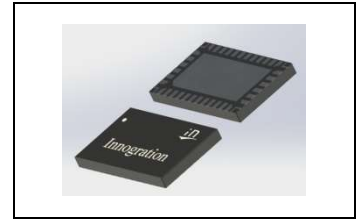




## 2.5-2.7GHz, 100W, 50V GaN Doherty PA Module

### Description

The SMAV2527-100 is a 100-watt, integrated 2-stage Power Amplifier Module, designed for 5G massive MIMO applications, with frequencies from 2.5 to 2.7GHz. The module is 50 Ω input fully matched and output partially matched, and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions, with much less sensitivity for production, housed in 10\*6mm cost effective plastic open cavity package, and heat dissipated by copper flange.



The module incorporates advanced Doherty circuit delivering high power added efficiency for the entire module at 16 W average power according to normal 8 dB back off.

**Innogrations owns the patents for internal Doherty architecture, and related plastic open cavity.**

- Typical Performance of Doherty Demo (On Innogrations fixture with device soldered through grounding vias):  
VDS= 50V, IDQ-main=63mA Vgs-main=-2.89V. Vgs-peak=-5.2V, Idq-driver=22mA, Vgs-Driver=-3.08V

Freq (GHz)	Pulse CW Signal(1)			Pavg=42dBm WCDMA Signal(2)		
	P1dB-Gain (dB)	P5dB (dBm)	P5dB (W)	Gp (dB)	Eff (%)	ACPR5M (dBc)
2.5	30.0	50.30	107	29.4	51.7	-27.1
2.6	31.4	50.22	105	30.7	50.8	-28.7
2.7	31.7	50.0	100	30.8	49.3	-31.8

Notes:

(1) Pulse Width=100 us, Duty cycle=20%

(2) WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz, PAR =10.5 dB at 0.01 % probability on CCDF.

### Features and Benefits

- Adjustable drain bias to fit different power demand
- Extremely good VBW performance to enable the broadest IBW/OBW
- Industry leading RF performance for 5G MIMO AAU, for instance
  - ✓ 32T:320W
- Plastic open cavity without molding compound brings advantage compared to molded design
  - ✓ Minimize the risk of high density thermal distribution in fanless system for longer life time
  - ✓ Highly consistent RF performance for yield of volume production
- 50 Ω Input matched, output partially matched, effective PCB space smaller than 12\*20mm
- Integrated Doherty Final and driver Stage
- 6x10 mm Surface Mount Package, full copper flange underneath for grounding and heat dissipation, much more effective than LGA PCB based design

### Pin Configuration and Description





Pin No.	Symbol	Description
6	RF IN	RF Input
1	VDS-driver	Driver stage, Drain Bias
4	VGS-driver	Driver stage, Gate Bias
19,21	RF Out2	RF Output, Drain Bias of Main Amplifier
22,24	RF Out1	RF Output, Drain Bias of Peaking Amplifier
11	VGS-main	Main Amplifier, Gate Bias
32	VGS-peak	Peaking Amplifier, Gate Bias
3,8-10,14,15,16,17,26,27,28,29,33-35	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36	GND	Internal Grounding, recommend connecting to Epad ground
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	200	Vdc
Gate--Source Voltage	$V_{GS}$	-8 to +0.6	Vdc
Operating Voltage	$V_{DD}$	+60	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_j$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance@Average Power, Junction to Case $T_{case}=+85^{\circ}C$ , CW Test, $P_{out}=16W$ ,	$R_{\theta JC}$	2.8	°C/W

Notes:

- (1) The thermal resistance is acquired by our company's FEA model, which was calibrated by IR measurement, the value shall be applied to reliability.
- (2) The reference  $T_{case}$  temperature  $85^{\circ}C$  is apply on the backside of package.
- (3) If the device soldering onto the 20mil Rogers PCB with  $108 \times \Phi 0.25mm$  via hole beneath the package backside and the reference temperature  $T_{case}$  ( $85^{\circ}C$ ) apply on the groundside of the PCB, the total thermal resistance  $R_{\theta JC}$  (TBD)°C/W.
- (4) The power dissipation in the table is overall dissipation which includes Carrier PA, Peaking PA and driver PA.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class Voltage
Human Body Model(HBM) (JEDEC Standard JESD-A114)	TBD
Charged Device Model (CDM) (JEDEC Standard JESD22-C101F)	$\pm 1000V$

**Table 4. Electrical Characteristics**

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		2.5		2.7	GHz
Driver Quiescent Current ( $I_{DQ-driver}$ )			22		mA
Carrier Quiescent Current ( $I_{DQ-main}$ )			63		mA
Peak PA Gate Quiescent Voltage ( $V_{PEAK}$ )			-5.3		V
Power Gain @ $P_{out}=42dBm$	Freq=2.6GHz		30		dB
Efficiency @ $P_{out}=42dBm$	Freq=2.6GHz		50		%
$P_{peak}$ by CCDF	Freq=2.6GHz		100		W



Load Mismatch of per Section (On Test Fixture, 50 ohm system):  $f = 2.6\text{GHz}$

VSWR 10:1 at P5dB pulse CW Output Power	No Device Degradation
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## TYPICAL CHARACTERISTICS

Application board and its layout info based on request

Figure 1. Power Gain and Drain Efficiency as Function of Pulsed CW Output Power

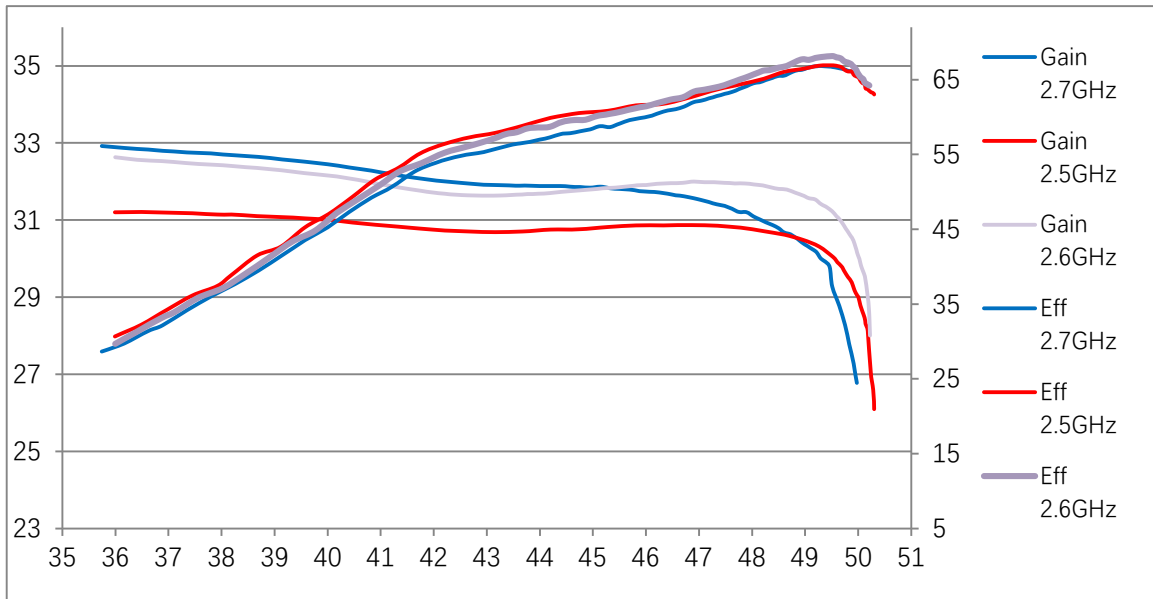


Figure 2. Network analyzer output S11/S21

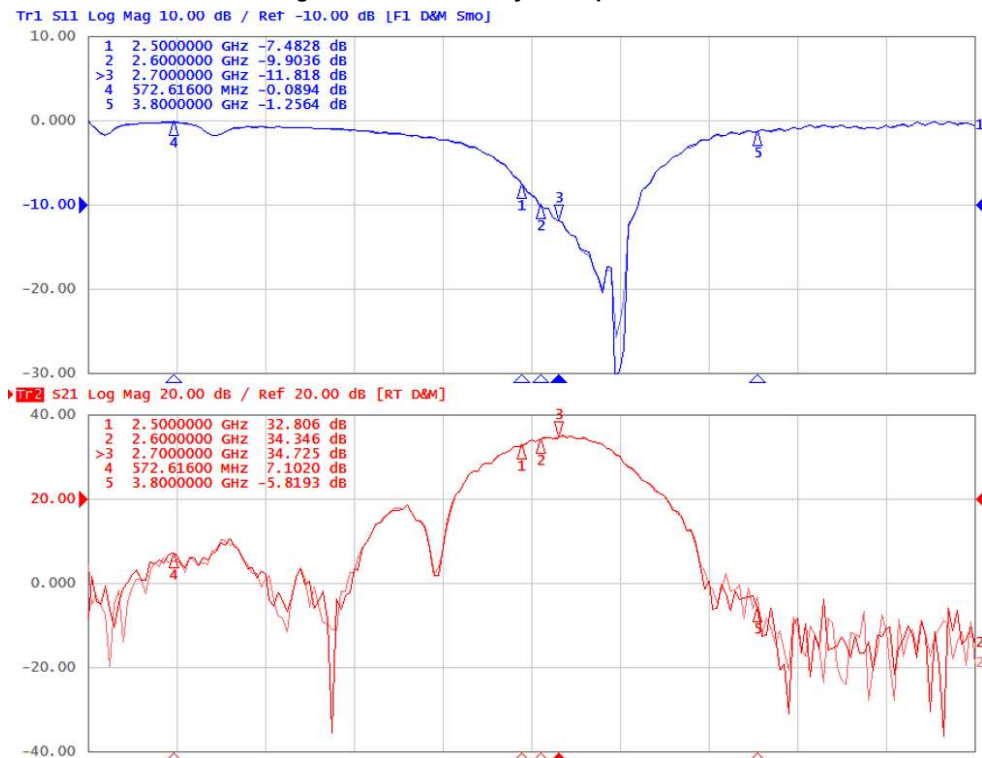


Figure 3. Video Impedance Test

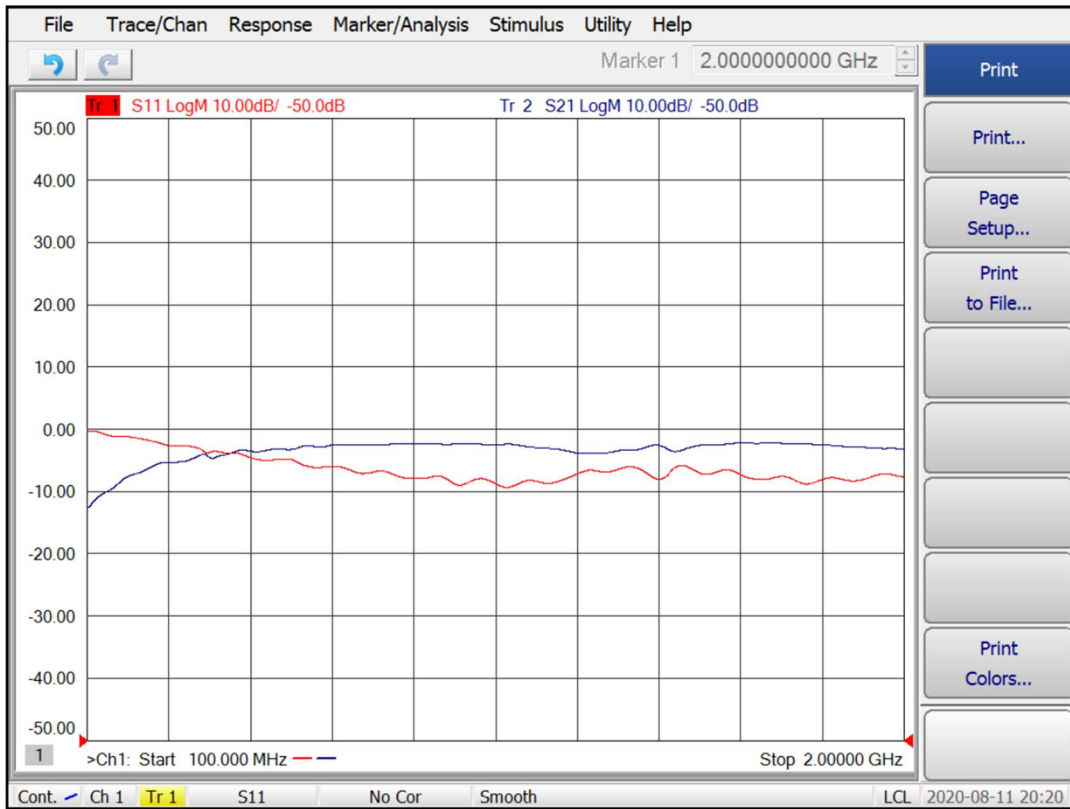
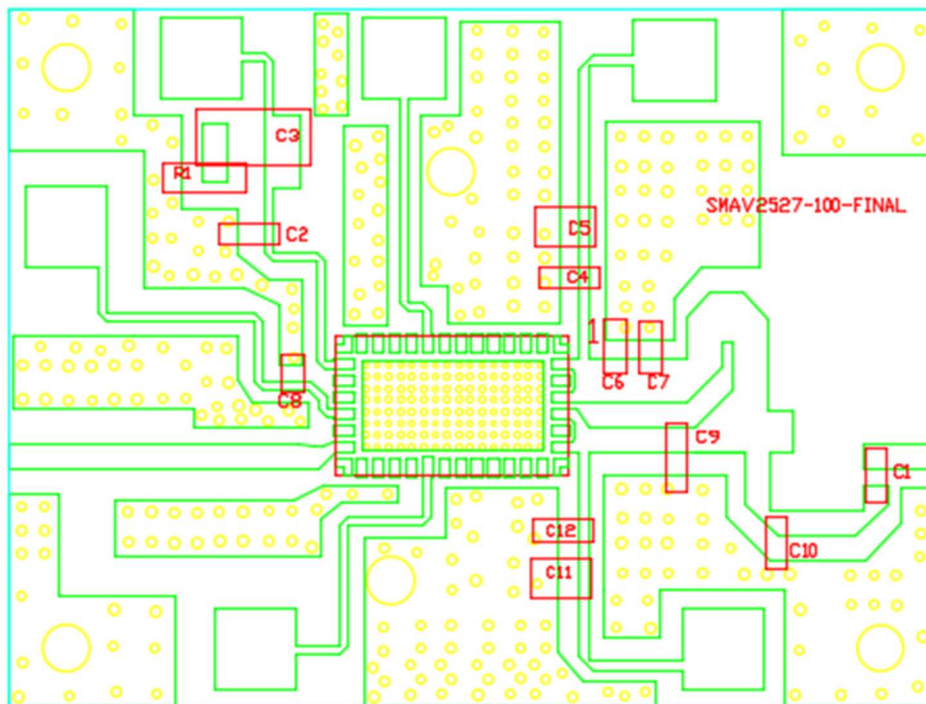


Figure 4. Application board layout info

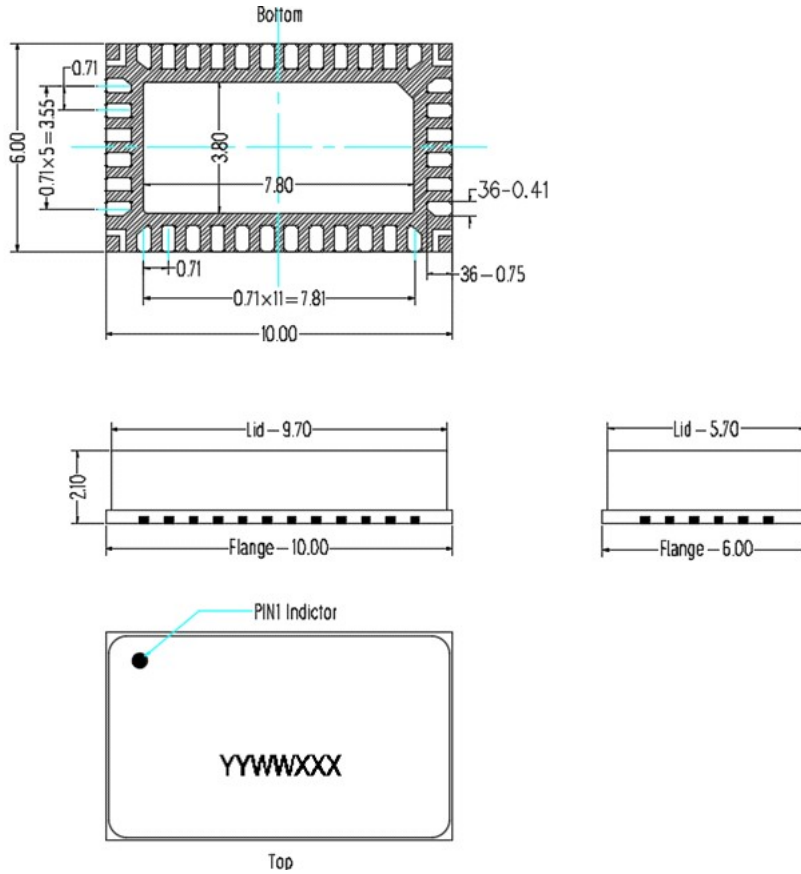




<b>BOM</b>				
<b>Part</b>	<b>Quantity</b>	<b>Description</b>	<b>Part Number</b>	<b>Manufacture</b>
C1,C2,C4,C12	4	10pFHigh Q Capacitor	251SHS100BSE	TEMEX
C6	1	1.6pFHigh Q Capacitor	251SHS1R6BSE	TEMEX
C7	1	1.2pFHigh Q Capacitor	251SHS1R2BSE	TEMEX
C8	1	1000pF	RS80R2A104M	TEMEX
C3,C5,C11	3	10uF MLCC	RS80R2A106M	MARUWA
C9	1	1.5pFHigh Q Capacitor	251SHS1R5BSE	TEMEX
C10	1	0.9pFHigh Q Capacitor	251SHS0R9BSE	TEMEX
R1	1	10 $\Omega$ Power Resistor	ESR03EZPF100	ROHM

## Package Dimensions

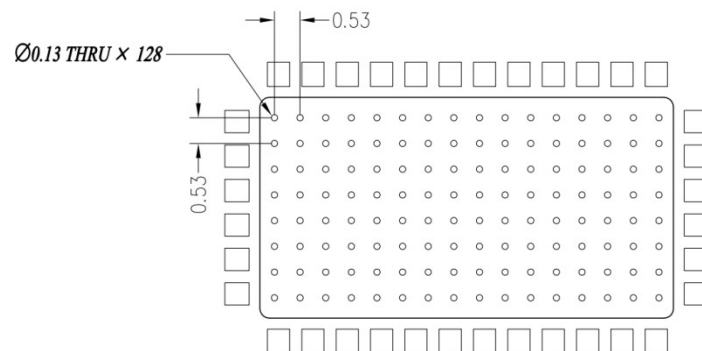
### 10\*6 Plastic Package



#### Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are  $\pm 0.2$ mm.

## Mounting Footprint Pattern



#### Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/12/16	Rev 1.0	Preliminary Datasheet
2022/3/30	Rev 1.1	Modified pins definition of drain bias for main and peak path

Application data based on LWH-21-13

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