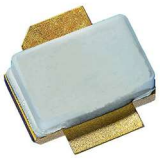
Gallium Nitride 50V, 45W,1-4GHz Full band RF Power Transistor

Description

SU4005VS



The SU4005VS is a single ended 45W, GaN HEMT, ideal for full band applications from 1 to 4GHz. It can support pulsed amplifier or back off linear amplifier, **but NOT suitable** for CW operation due to thermal limitation.

- Typical performance across 1-4GHz with device soldered
  VDS = 50 V, IDQ=25mA,100us, 10% duty cycle

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
1000	37.6	47.91	61.80	0.216	10.31	57.22
1200	38.7	47.78	59.98	0.239	9.08	50.19
1400	38.4	47.96	62.52	0.25	9.56	50.01
1600	38.3	48.26	66.99	0.247	9.96	54.24
1800	38.7	47.89	61.52	0.221	9.19	55.67
2000	39	47.9	61.66	0.206	8.9	59.86
2200	38.7	47.29	53.58	0.175	8.59	61.23
2400	39.4	47.7	58.88	0.25	8.3	47.11
2600	39.2	47.77	59.84	0.264	8.57	45.33
2800	38.8	48.16	65.46	0.272	9.36	48.14
3000	38.7	48	63.10	0.288	9.3	43.82
3200	39	47.8	60.26	0.279	8.8	43.19
3400	39.1	47.67	58.48	0.271	8.57	43.16
3600	38.7	48.1	64.57	0.26	9.4	48.73
3800	39.3	47.1	51.29	0.26	7.8	40.2
4000	39.2	47.07	50.93	0.26	7.87	40.1

Applications

- L, S band narrow band pulsed power amplifier
- Ultrawide band power amplifier covering L+S band
- DAS or Jammer for 4G/5G

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	8	mA

Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, Pout=50W Pulsed CW	$R_{\theta JC}$	TBD	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (one path,measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=8mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 8mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=25mA, Measured in Functional Test	$V_{GS(Q)}$		-3.44		V

Figure 2: Median Lifetime vs. Channel Temperature

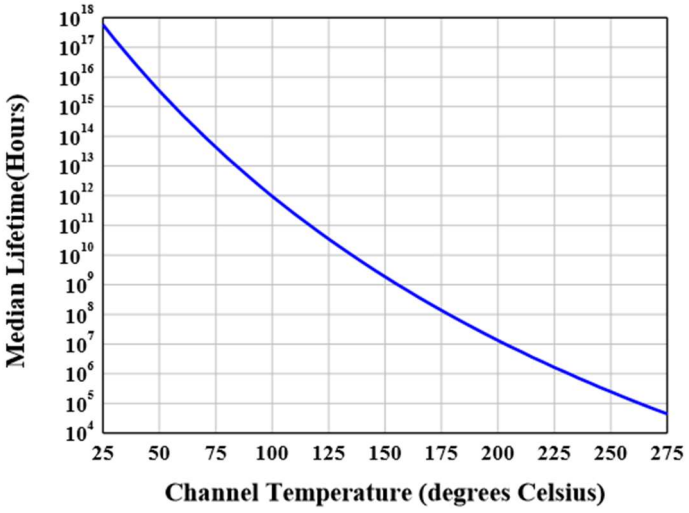


Figure 3: Network analyzer output, S21 (VDS=50V VGS=-3.31V IDQ=55mA)

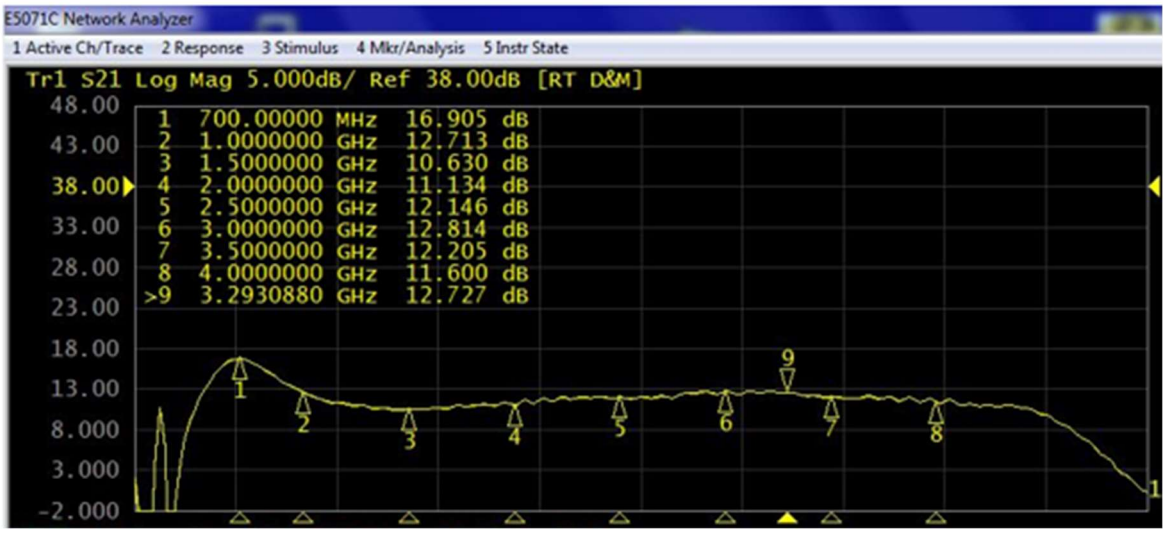


Figure 4: Picture of wide band application board (1-4GHz)

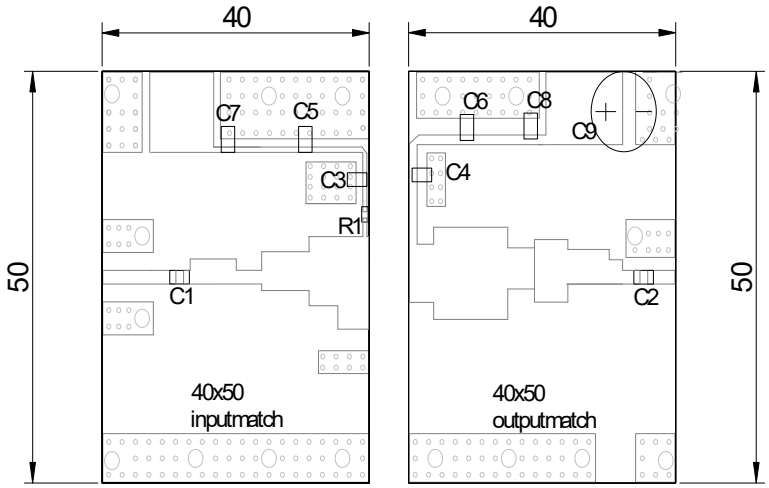
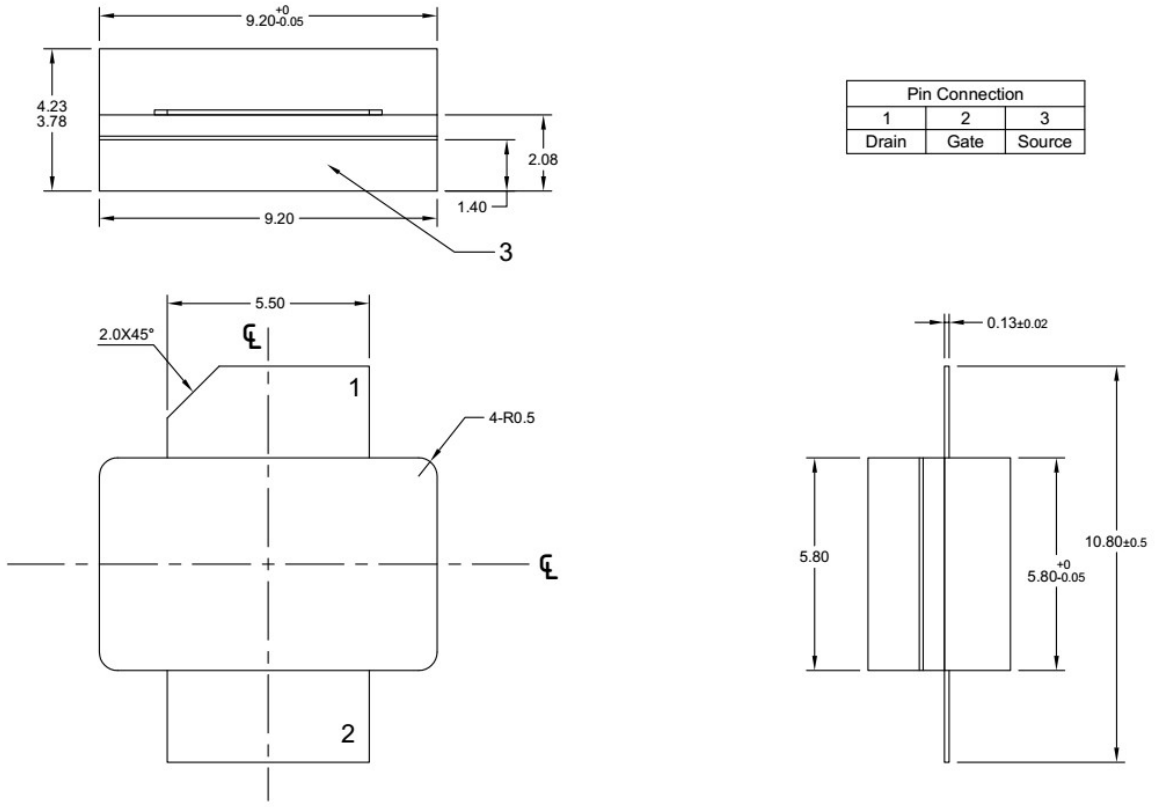


Table 4. Bill of materials of application board (PCB layout upon request)

Component	Description	Suggested Manufacturer
C1,C5,C6	20pF	ATC800B
C2,	20pF	ATC800R
C3,C4	100pF	ATC600F
C7,C8	Ceramic multilayer capacitor, 10uF, 100V	10uF/100V
C9	470UF	63V/470UF
R1	Chip Resistor,11Ω,0603	
PCB	0.762mm [0.020"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper	

Package Outline

Flanged ceramic package; 2 leads



Pin Connection		
1	2	3
Drain	Gate	Source

Unit: mm
Tolerances(unless specified): x.x ±0.25
x.xx ±0.13

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB-2EL-9.2					2018.1.31

Figure 2. Package Outline PKG-G2

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/4/11	V1.0	Preliminary datasheet creation

Application data based on YHG-21-04

Notice