# MM10R5E LDMOS TRANSISTOR

Document Number: MM10R5E
Product Datasheet V1.0

## 5W, 3.5GHz General Purpose RF LDMOS FETs

**MM10R5E**

### Description

The MM10R5E is a 5-watt, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies up to 3.5GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

It can support CW, pulsed CW either saturated or linear operation.

- Typical RF Performance within 2.5-2.7GHz (On Innogration fixture with device soldered):

$V_{DD}$ = 28 Volts, $I_{DQ}$ = 50 mA, Pulsed CW(20us, 10%)

| Freq (MHz) | P1dB (dBm) | P1dB (W) | P1dB Eff(%) | P1dB Gain(dB) | P3dB (dBm) | P3dB (W) | P3dB Eff(%) |
|---|---|---|---|---|---|---|---|
| 2500 | 38.85 | 7.7 | 56.9 | 17.72 | 39.57 | 9.1 | 59.5 |
| 2600 | 38.28 | 6.7 | 60.6 | 18.48 | 39.14 | 8.2 | 62.7 |
| 2700 | 37.38 | 5.5 | 55.9 | 18.36 | 38.44 | 7.0 | 59.2 |

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

### Suitable Applications

- General purpose power amplifier
- L, S band power amplifier

**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain--Source Voltage | $V_{DSS}$ | +65 | Vdc |
| Gate--Source Voltage | $V_{GS}$ | -10 to +10 | Vdc |
| Operating Voltage | $V_{DD}$ | +32 | Vdc |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Case Operating Temperature | $T_C$ | +150 | °C |
| Operating Junction Temperature | $T_J$ | +225 | °C |

**Table 2. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case<br>$T_C$= 85°C, $T_J$=200°C, DC test | $R_{\theta JC}$ | 6.5 | °C/W |

**Table 3. ESD Protection Characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JESD22--A114) | Class 2 |

**Table 4. Electrical Characteristics** (TA = 25 ℃ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DC Characteristics** | | | | | |
| Drain-Source Voltage<br>$V_{GS}$=0, $I_{DS}$=500uA | $V_{(BR)DSS}$ | 65 | 70 | | V |
| Zero Gate Voltage Drain Leakage Current<br>($V_{DS}$ = 50V, $V_{GS}$ = 0 V) | $I_{DSS}$ | —— | —— | 1 | μA |
| Zero Gate Voltage Drain Leakage Current<br>($V_{DS}$ = 28 V, $V_{GS}$ = 0 V) | $I_{DSS}$ | —— | —— | 1 | μA |
| Gate--Source Leakage Current<br>($V_{GS}$ = 9 V, $V_{DS}$ = 0 V) | $I_{GSS}$ | —— | —— | 1 | μA |
| Gate Threshold Voltage<br>($V_{DS}$ = 28V, $I_D$ = 600 μA) | $V_{GS(th)}$ | —— | 2 | —— | V |
| Gate Quiescent Voltage<br>($V_{DD}$ = 28 V, $I_D$ = 50 mA, Measured in Functional Test) | $V_{GS(Q)}$ | —— | 2.7 | —— | V |
| Common Source Input Capacitance<br>($V_{GS}$ = 0V, $V_{DS}$ =28 V, f = 1 MHz) | $C_{ISS}$ | | 8 | | pF |
| Common Source Output Capacitance<br>($V_{GS}$ = 0V, $V_{DS}$ =28 V, f = 1 MHz) | $C_{OSS}$ | | 3 | | pF |
| Common Source Feedback Capacitance<br>($V_{GS}$ = 0V, $V_{DS}$ =28 V, f = 1 MHz) | $C_{RSS}$ | | 0.2 | | pF |

**Load Mismatch (In Innogration Test Fixture, 50 ohm system):** $V_{DD}$ = 28 Vdc, $I_{DQ}$ = 50 mA, f = 2700 MHz

| | |
|---|---|
| VSWR 10:1 at 20W pulse CW Output Power | No Device Degradation |

## TYPICAL CHARACTERISTICS

**Figure 1. Network analyzer output S11/S21**

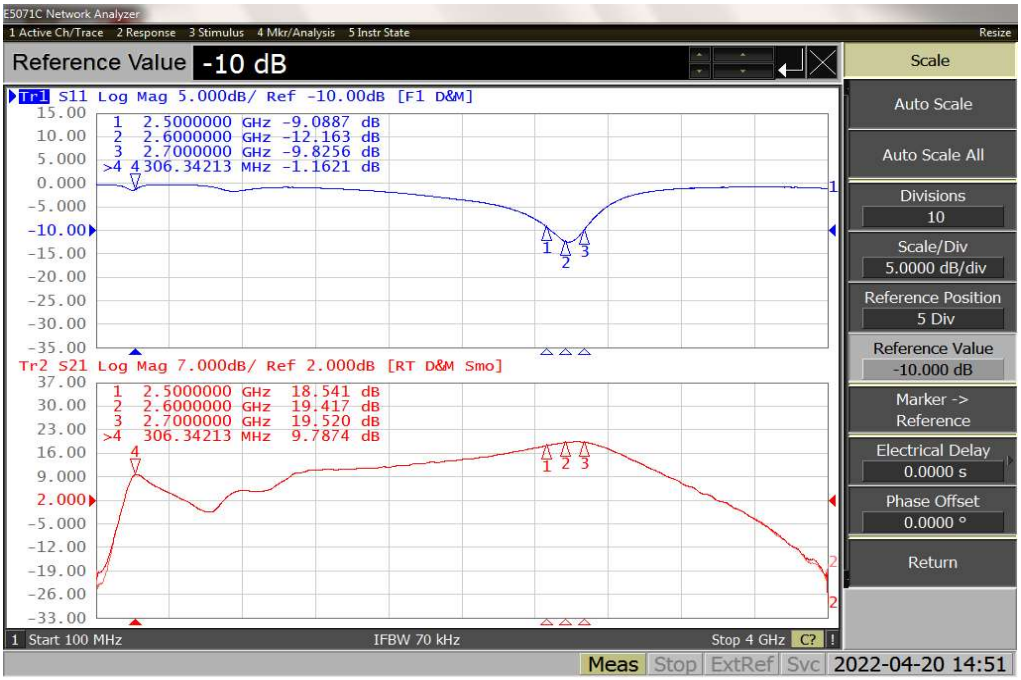


**Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power**

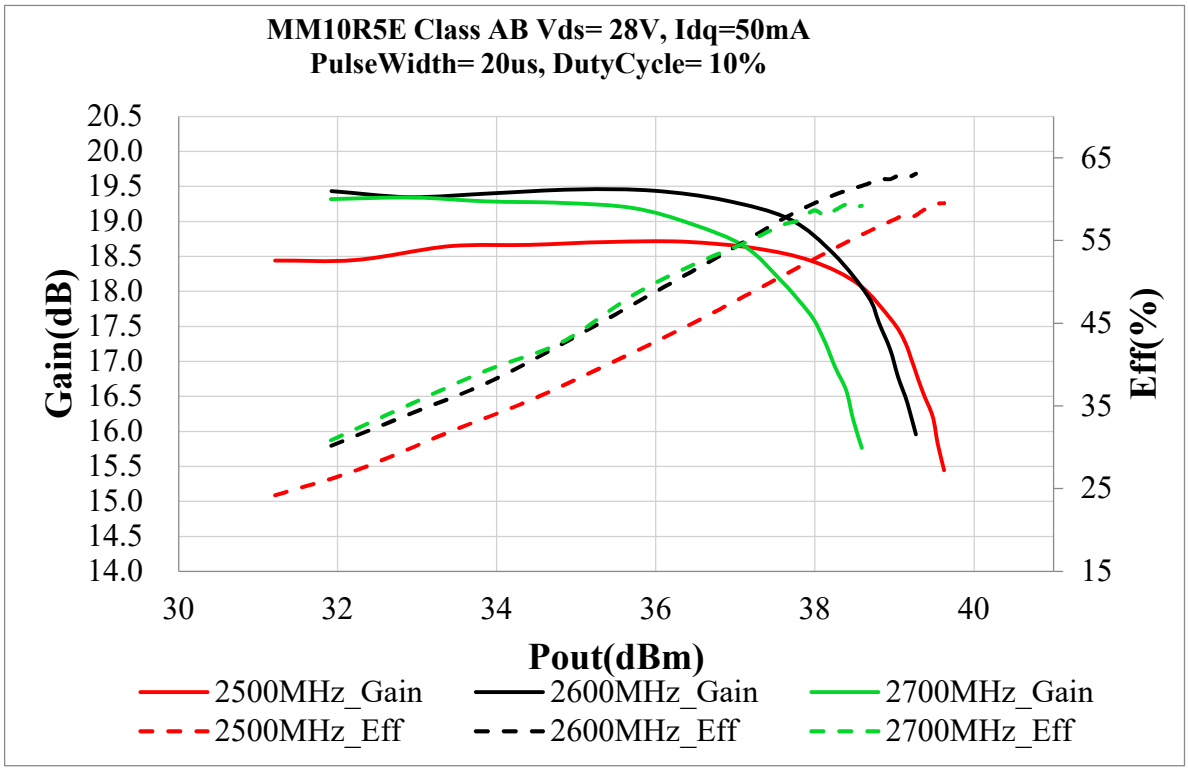



**Figure 3. Test Circuit Component Layout** (PCB: 20 Mils, RO4350B）

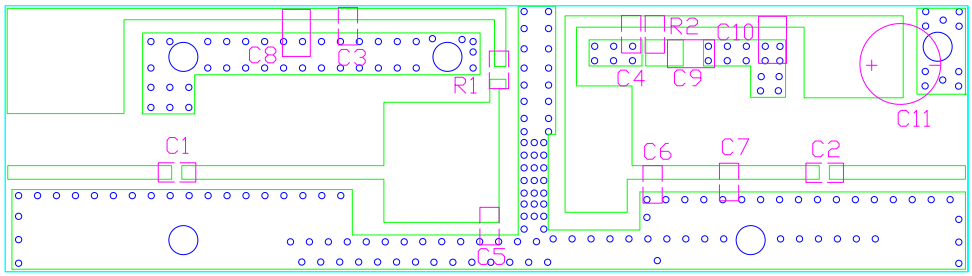
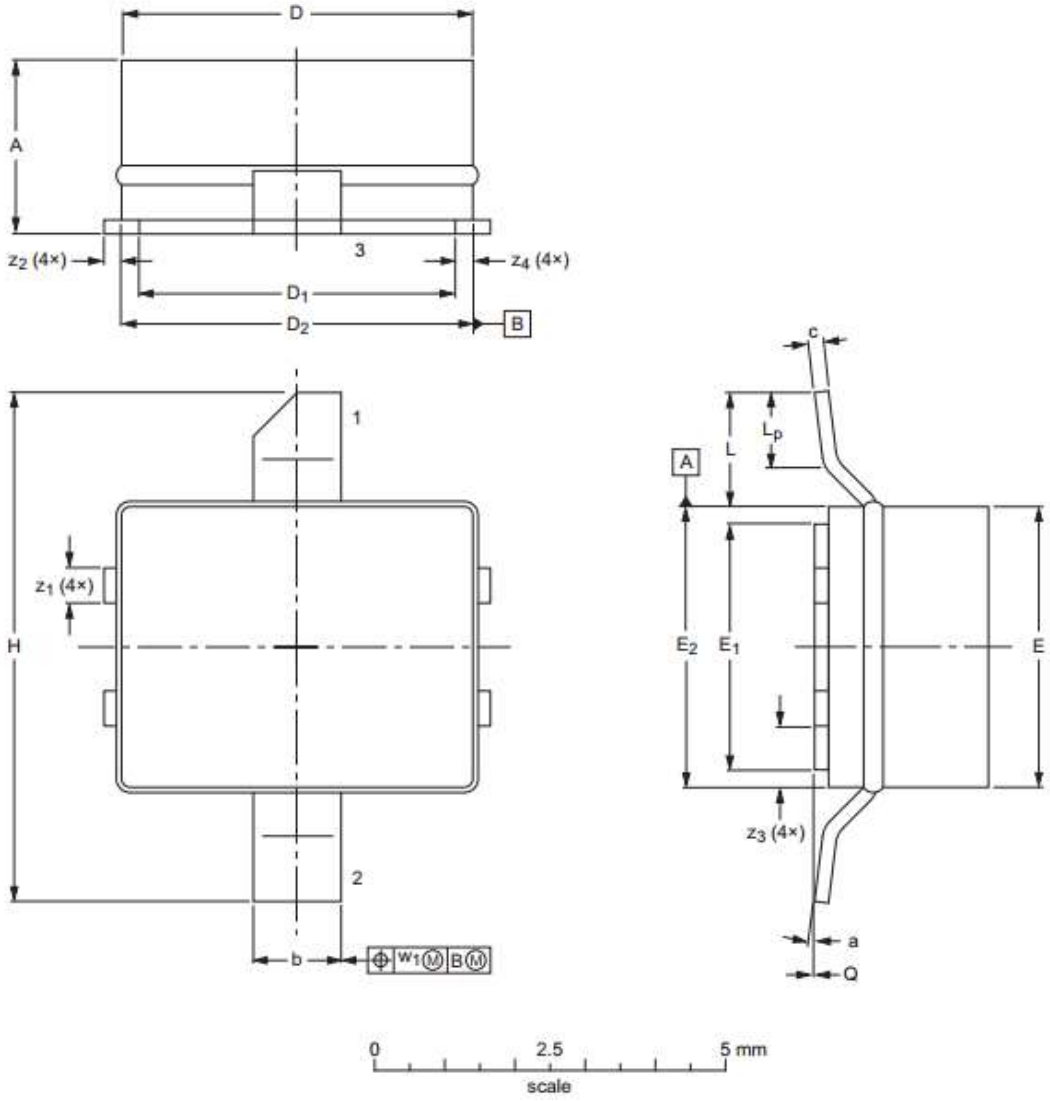



**Table 4. Test Circuit Component Designations and Values**

| Designator | Comment | Footprint | Quantity |
|---|---|---|---|
| C1, C6 | 2.2 pF | 0603 | 2 |
| C2, C3, C4 | 12 pF | 0603 | 3 |
| C5, C7 | 1.0 pF | 0603 | 2 |
| C8, C9, C10 | 10 uF/100V | 1210 | 3 |
| C11 | 100 uF/50V | | 1 |
| R1, R2 | 10 Ω | 0603 | 2 |

## Package Outline

**Earless Flanged ceramic package; 2 leads(1-Drain,2-Gate,3-Source)**




| UNIT | A | b | c | D | $D_1$ | E | $E_1$ | $E_2$ | H | L | $L_P$ | Q | $w_1$ | $z_1$ | $z_2$ | $z_3$ | $z_4$ | α |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.34 | 1.35 | 0.23 | 5.16 | 4.65 | 4.14 | 3.63 | 4.14 | 7.49 | 2.03 | 1.02 | 0.1 | 0.25 | 0.58 | 0.25 | 0.97 | 0.51 | 7° |
| | 2.13 | 1.19 | 0.18 | 5.00 | 4.50 | 3.99 | 3.48 | 3.99 | 7.24 | 1.27 | 0.51 | 0.0 | | 0.43 | 0.18 | 0.81 | 0.00 | 0° |

| OUTLINE VERSION | REFERENCE | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | |
| PKG-MM | | | | | 18/6/2014 |

## Revision history

**Table 5. Document revision history**

| Date | Revision | Datasheet Status |
|---|---|---|
| 2022/4/20 | Rev 1.0 | Product Datasheet |
| | | |
| | | |

**Application data based on LSM-22-06**

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