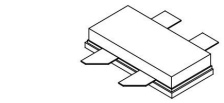
700MHz-1000MHz, 140W, 28V High Power RF LDMOS FETs

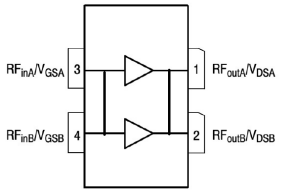
Description

The ITCH09140B2-R1 is a 140-watt, internally matched LDMOS FET, designed for CDMA/WCDMA and multicarrier GSM base station applications with frequencies from 700 to 1000 MHz. It can be used in Class AB/B and Class C for all typical cellular base station modulation formats.

Due to internal connections at input and output, it must be used as single-ended configuration.

ITCH09140B2-R1





(Top View)

•Typical Single-Carrier W-CDMA Performance: V_{DD}=28Volts, I_{DQ}= 1100mA

P_{out}=42dBm							
Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Efficiency (%)
758	42.00	10.04	52.04	160.0	-38.5	21.3	21.0
780	42.01	9.57	51.58	144.0	-40.8	22.1	22.9
803	42.00	9.27	51.27	134.1	-41.9	21.0	23.8

•Typical Pused CW Performance: V_{DD}=28Volts, I_{DQ}= 1100mA

Pulsed conditions: 20uS width，10% dule cycle

Freq (MHz)	P1dB(dBm)	P1dB(W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB(dBm)	P3dB(W)	P3dB Eff(%)
758	52.22	166.8	59.1	19.7	53.14	206.0	64.7
780	51.69	147.6	63.3	20.03	52.51	178.1	67.7
803	50.81	120.4	61.1	19.57	51.79	151.1	65.6

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	65	70		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate—Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 1 Ma)	$V_{GS(th)}$		2.2		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_{DQ} = 1100 Ma, Measured in Functional Test)	$V_{GS(Q)}$	2.6	3.08	3.6	V
Functional Tests (In Innogration Test Fixture, 50 ohm system) : V_{DD} = 28 Vdc, I_{DQ} = 1100 mA, f = 780 MHz, Pulse CW Signal Measurements. (Pulse Width=20 μs, Duty cycle=10%)					
Power Gain	G_p		20		Db
Drain Efficiency@P1dB	η_D		60		%
1 Db Compression Point	P_{-1Db}		140		W
Input Return Loss	IRL		-7		Db

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 1100 mA, f = 780 MHz

VSWR 10:1 at 140W pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

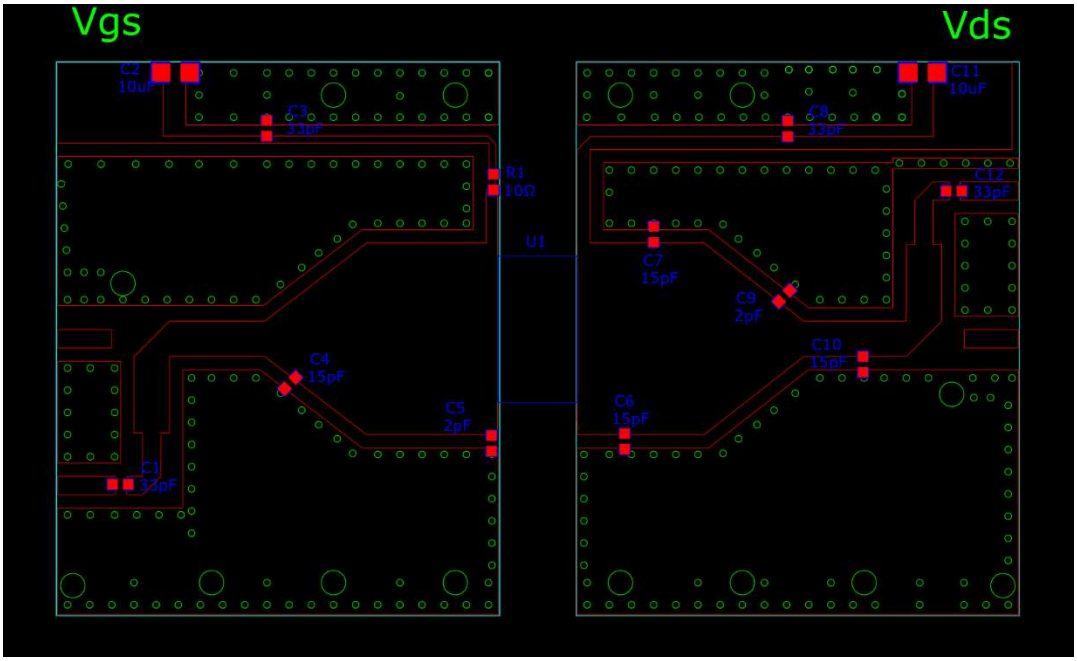


Figure 1. ITCH09140B2-R1 Test Circuit Component Layout(758MHz~803MHz)

Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
U1	ITCH09140B2-R1	1
C1、C3、C8、C12	33Pf	4
C4、C6、C7、C10	15Pf	4
C5、C9	2Pf	2
C2、C11	10Uf	2
R1	10Ω	1
PCB	Roger 4350B 30mils	

TYPICAL CHARACTERISTICS

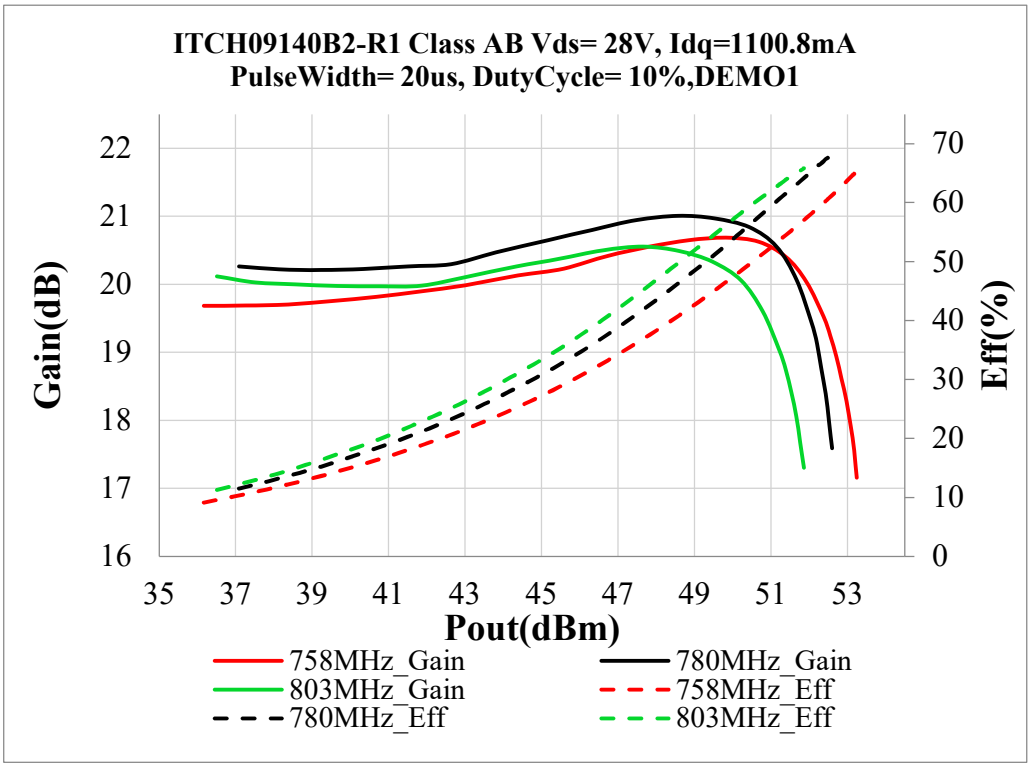


Figure 2. Power gain and drain efficiency as function of pulsed CW Pout

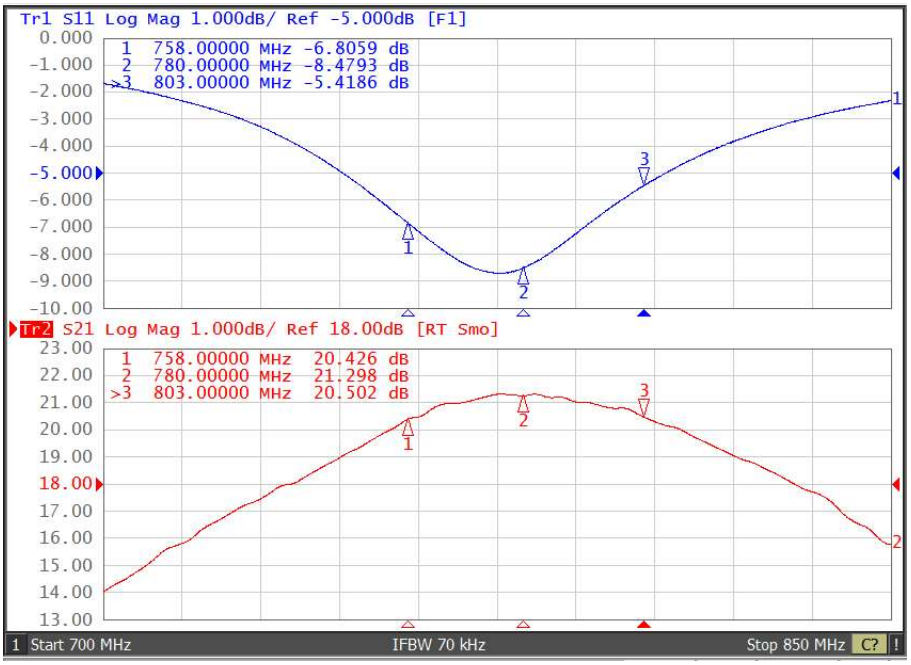
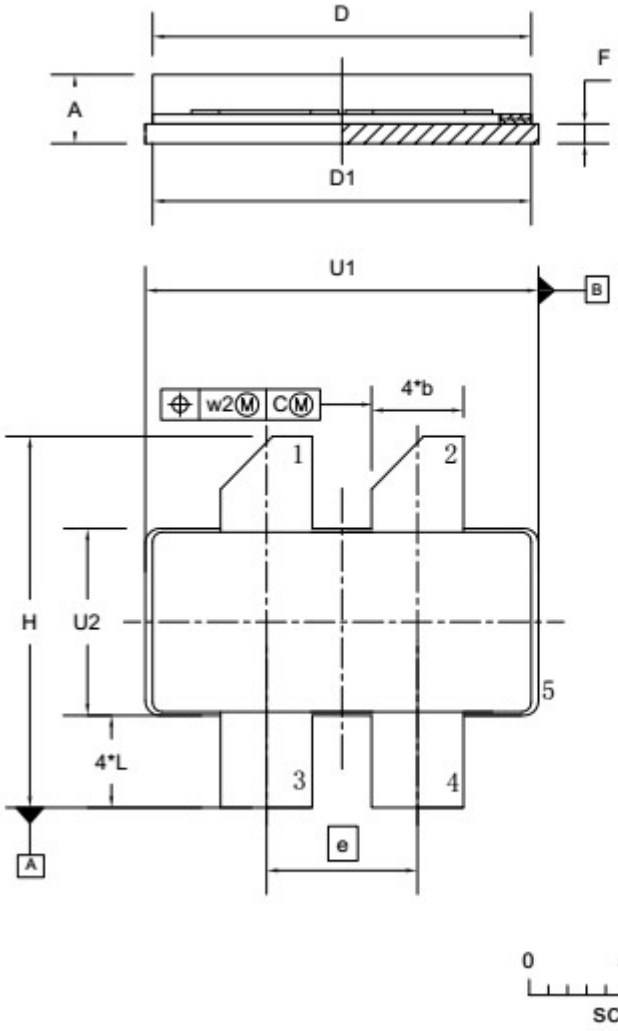


Figure 3. Broadband Frequency Response

Package Outline

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	F	H	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.93 4.67	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2-R1					03/12/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2022/4/29	Rev 1.0	Product Datasheet

Application data based on ZYX-22-04

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