MK3114C LDMOS TRANSISTOR

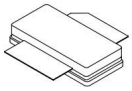
Document Number: MK3114C
Preliminary Datasheet V1.1

2700MHz-3100MHz, 140W, 32V High Power RF LDMOS FETs

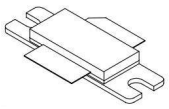
Description

The MK3114C is a 140-watt, internally matched LDMOS FETs, designed for RF System applications with frequencies at 2700 MHz to 3100MHz.It can be used in Class AB/B and Class C for all pulsed CW formats.

MK3114CS



MK3114C



- Typical Performance (on wideband board with device soldered):

VDD = 32 Volts, I_{DQ} = 100 mA, Pulse Width =300us,Duty Cycle =15%.

Freq(MHz)	G_P(dB)	P_{1dB}(W)	η_D(%)
2700	12.2	162	48.5%
2900	12.6	164	49.5%
3100	12.1	148	47.5%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 140 W Pulsed, 32 Vdc, I_{DQ} = 100 mA	$R_{\theta JC}$	0.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (VDS = 65V, VGS = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (VDS = 32 V, VGS = 0 V)	I_{DSS}			1	μA

Gate--Source Leakage Current (VGS = 6 V, VDS = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (VDS =32V, ID = 300 μA)	$V_{GS(th)}$		1.8		V
Gate Quiescent Voltage (VDD = 32 V, ID = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.3		V

Functional Tests (On Demo Test Fixture) VDD = 32Vdc, IDQ = 100 mA, f = 3100 MHz, pulse CW, Pulse Width =300us,Duty Cycle =15%.

Power Gain@P1dB	Gp		12.1		dB
Drain Efficiency@P1dB	η_D		47.5		%
1 dB Compression Point	P_{1dB}		148		W
Input Return Loss	IRL		-7		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 32 Vdc, I_{DQ} = 100 mA, f = 3100 MHz

VSWR 10:1 at 140W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

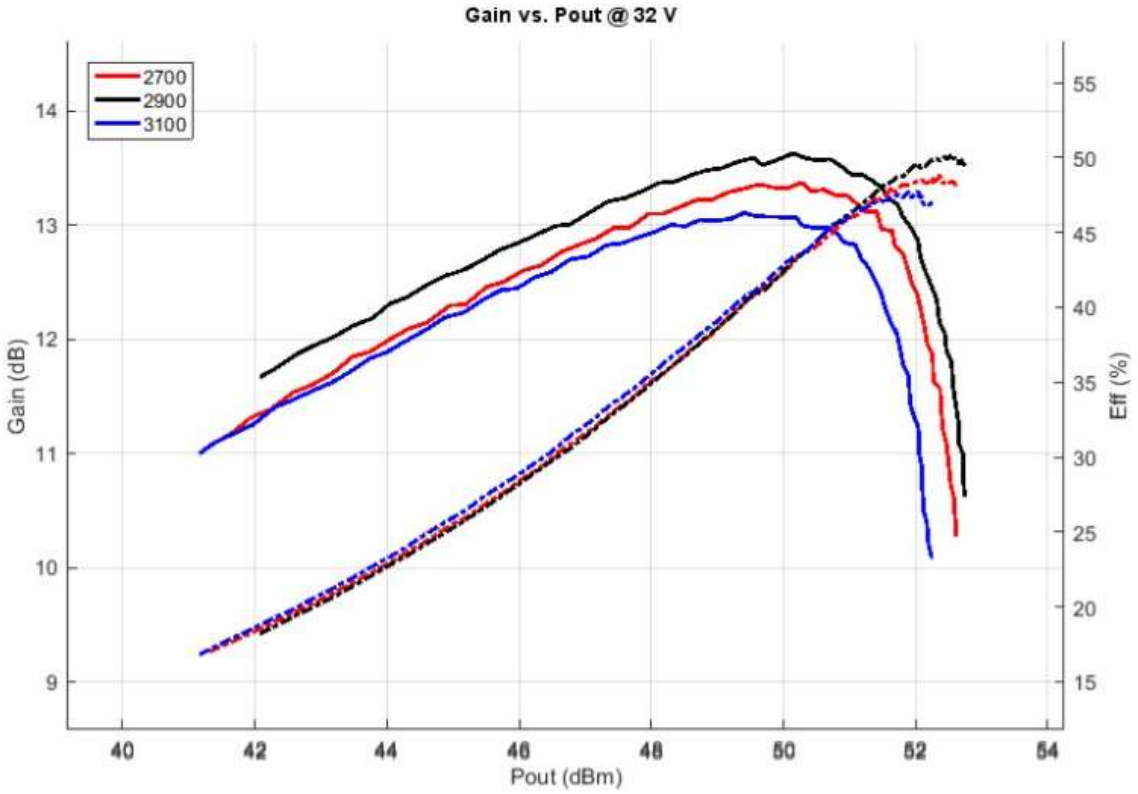
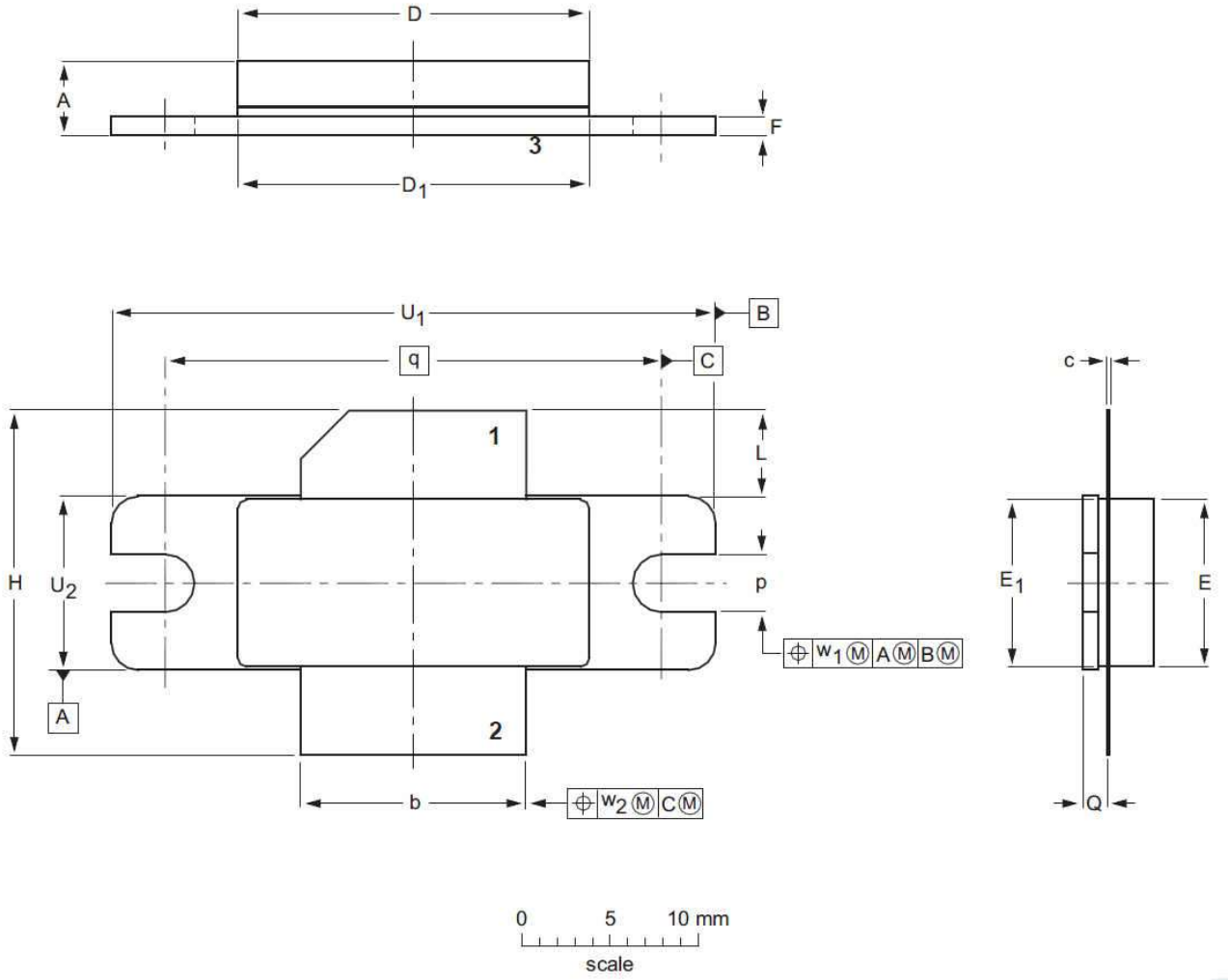


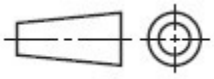
Figure 1. Power Gain and Drain Efficiency as Function of Pulse Output Power

Package Outline

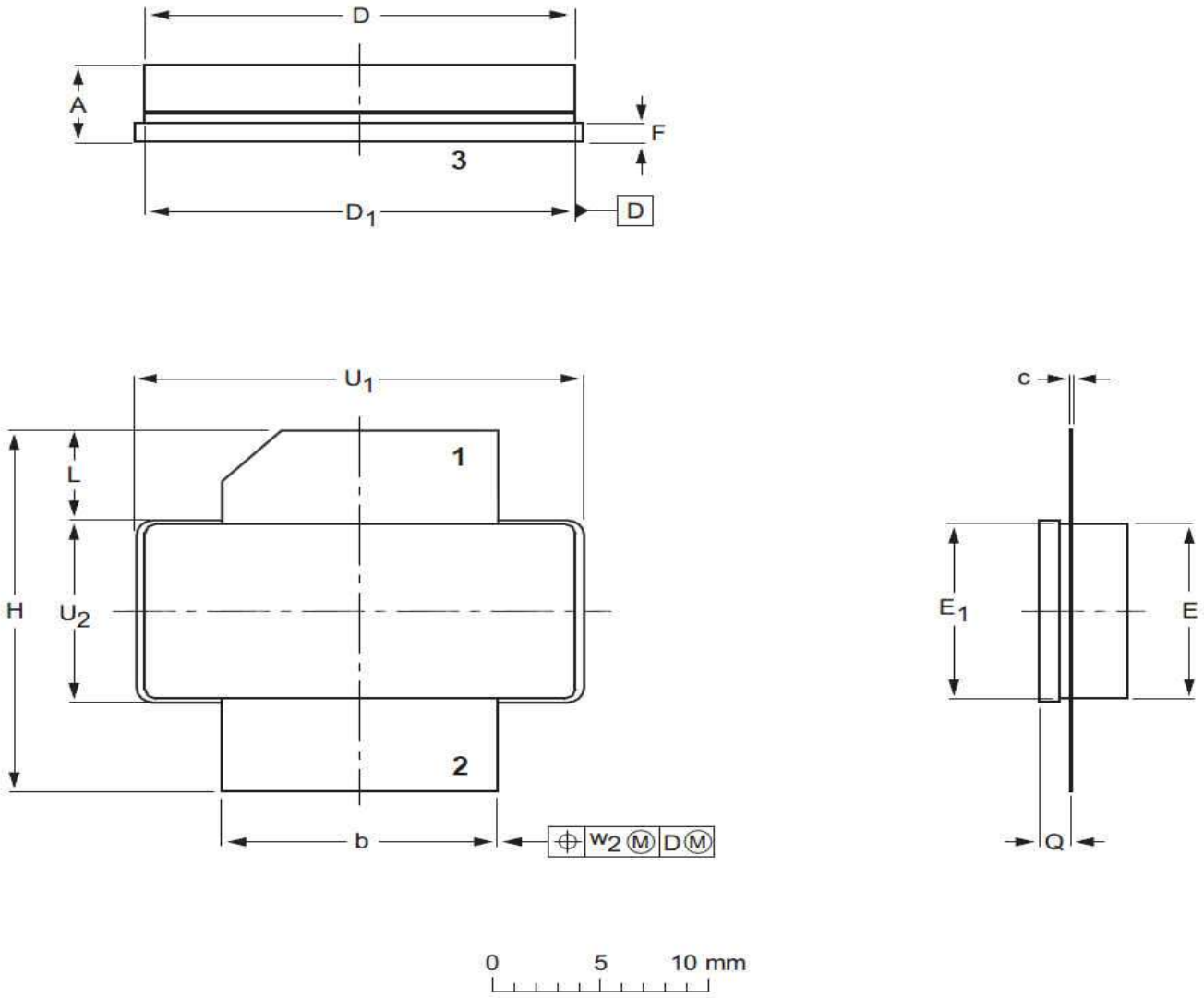
Flanged ceramic package; 2 mounting holes; 2 leads



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PKG-B2E						03/12/2013

Earless flanged ceramic package; 2 leads



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PKG-B2						03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/10/19	Rev 1.0	Preliminary Datasheet Creation
2022/5/10	Rev 1.1	Modification on 1st page, and Rj etc

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